Applied Telecom, Inc.

POINT

(PCI Optical Interface Network Transceiver)

Hardware Design Manual

Revision: 0.5

September 26, 1997

1. Introduction

This document details the hardware design of the PCI Optical Network Transceiver (POINT). The POINT is capable of sending and receiving data to/from optical data streams up to the full OC-12 bandwidth of 599040 Mbit/s. The board mounts into a standard full length PCI card slot and fully complies with the PCI revision 2.1 specification. POINT contains connectors for mounting of Applied Telecom's AIM family of interface modules. By utilizing AIM's, POINT can be configured for several standard Telecom interfaces including OC-12 and OC-3. Optical connections are made via convienent and economical duplex SC connectors. The POINT hardware design makes extensive use of FPGA technology to allow for maximum flexibility in sending or extracting data from the optical signal.

2. Functional Description

A block diagram of the POINT module is shown in Figure 1 below:
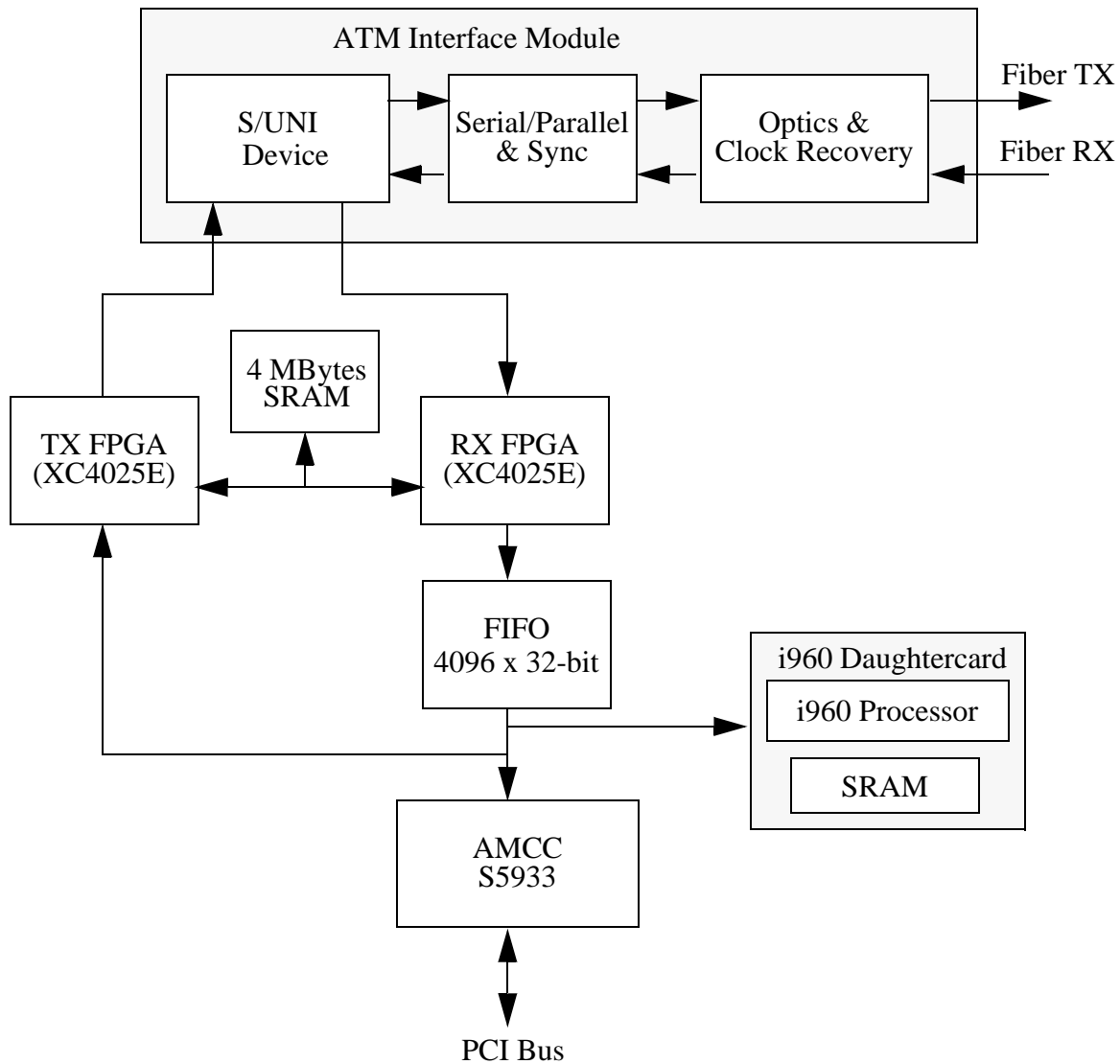
Figure 1. POINT High-Level Block Diagram

2.1 RX FPGA Circuit Description

The Receive FPGA is capable of operating in several different modes. Each mode requires a separate FPGA design and hence a separate bit file to download. Two modes have been defined: AAL5 mode and PPP mode.

2.1.1   AAL5 Mode

The basic function of the OC-12 PCI Module Receive FPGA when it is programmed in the AAL5 mode is to filter and pass specific portions of AAL5 ATM cells. In addition to these AAL5 cells, the PCI Module can be optioned to pass OAM/RM cells. When an ATM cell is received, it is first determined if the cell is an AAL5 data cell or an OAM/RM cell.

OAM/RM cells are identified by having PTI bit 2 set in the ATM header. If the FPGA detects that the PTI bit 2 is set, it will increment a 32-bit OAM/RM cell counter. It will then look at bit 4 in FPGA Control Register II to determine if it should pass the OAM/RM cell to the AMCC PCI controller (bit 4 = 1) or if it should discard the cell (bit 4 = 0). If bit 4 in the FPGA control register is set the FPGA will write the timestamp and ATM cell information to the AMCC PCI Controller.

AAL5 data cells are identified by having PTI bit 2 clear in the ATM header. The PCI Module will pass the beginning and optionally the last data cell of an AAL5 data stream for a particular VPI/VCI address. The number of cells passed at the beginning of the AAL5 data stream can be configured via a 2-bit TCNT value. This allows up to three cells to be passed from the start of an AAL5 data stream. Due to SRAM storage limitations, the PCI Module can only keep 2-bit counter values for a total of 2^{24} VPI/VCI unique addresses. Since the SRAMS are organized as 32 bit words, the counters are accessed using a 20-bit address and 4-bit index which points to 16 2-bit values within a 32-bit word. In NNI mode, the VPI expands to use the GFC bits to create a 12-bit VPI address. Thus, when combined with the 16-bit VCI address there can be a total of 2^{28} unique VPI/VCI addresses. To handle these extra 4 bits the PCI Module can select between the extended VPI or upper VCI bits and create a match mask to qualify the 'ignored' bits. The NNI Select bits determine the number of upper VCI bits to be replaced by the extended VPI bits. These bits form a 4-bit address field which is part of the 20 bit SRAM address. Table 1 shows how the SRAM address and index are created by the VPI/VCI bits.

The 'ignored bits' pass through a matching circuit. This matching circuit is controlled by an 8-bit match register. The lower four bits of this register contain the match value that gets compared against the ignored bits (extended VPI or upper VCI bits). The upper four bits of the match register contain enable bits that allow the user to enable/disable matching on a per bit basis. To disable the ignore bit matching function, simply disable matching for all four match value bits.

SRAM	VPC/VCI
A19	VPI bit 7
A18	VPI bit 6
A17	VPI bit 5
A16	VPI bit 4
A15	VPI bit 3
A14	VPI bit 2
A13	VPI bit 1
A12	VPI bit 0
A11	VCI bit 15 or VPI bit 8
A10	VCI bit 14 or VPI bit 9
A9	VCI bit 13 or VPI bit 10
A8	VCI bit 12 or VPI bit 11
A7	VCI bit 11
A6	VCI bit 10
A5	VCI bit 9
A4	VCI bit 8
A3	VCI bit 7
A2	VCI bit 6
A1	VCI bit 5
A0	VCI bit 4
Index3	VCI bit 3
Index2	VCI bit 2
Index1	VCI bit 1
Index0	VCI bit 0

Table 1: SRAM Address/Index Creation

The following diagram shows the matching logic for a single bit:
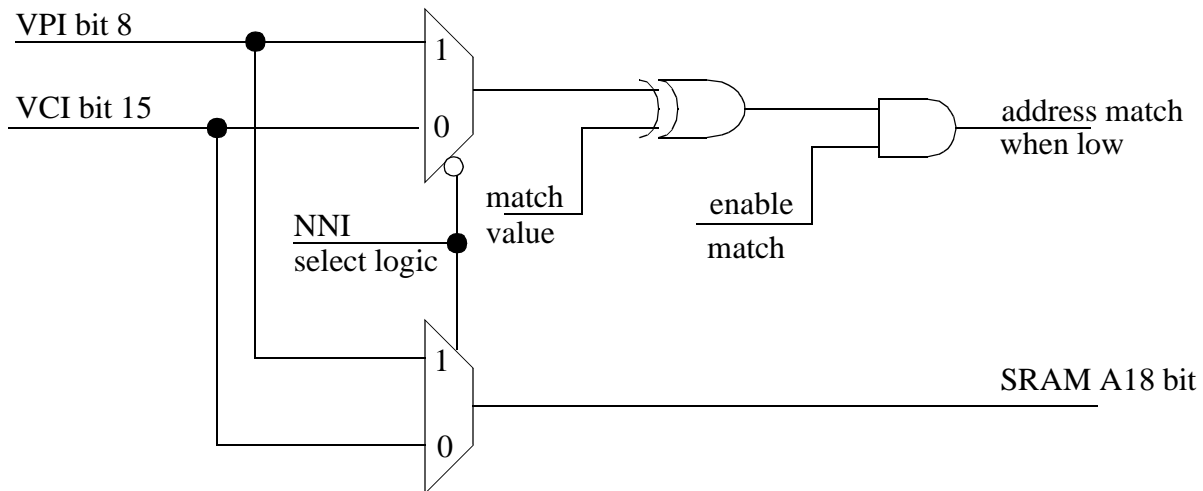
If the ignored bit address does not match, the 32-bit Unmatched NNI Cell Counter is incremented and the cell is discarded.

The OAM/RM Cell Counter and the Unmatched NNI Cell Counter are controlled via the Cell Count Transfer/Reset control bit. This bit is used to transfer count values to a read register and to reset the counters back to zero. These counters must be polled by software before a counter rollover can occur. Assuming every cell read from the AIM is a valid cell to count (worse case analysis) requires each cell counter to be read at least once every 2900 seconds (48.3 minutes).

Once the qualified VPI/VCI address is created, the FPGA will read SRAM memory to access the current 2-bit count value for that address. The FPGA will then look at PTI bit 1. If this bit is clear and the PASSALL control bit is clear, the 2-bit count value is read from SRAM. If the 2-bit count value is less than TCNT, the cell timestamp/2-bit count value, cell header, and/or cell payload will be sent to the AMCC PCI controller (as configured via control bits) and the count value incremented by one. If the 2-bit count value is equal to TCNT, the cell is discarded and the count value is not incremented. If the PTI bit 1 is clear and the PASSALL control bit is set, the cell timestamp/2-bit count value, cell header, and/or cell payload will be sent to the AMCC PCI controller and the count value will be incremented but limited to TCNT. If PTI bit 1 is set, this will indicate that this is the last cell for that particular address. If bit 5 of Control Register II is set, the cell timestamp/2-bit count value (equal to TCNT), cell header, and/or cell payload will be sent to the AMCC PCI controller and the count value will be reset to zero. If bit 5 of Control Register II is clear, the cell will be discarded and the count value will be reset to zero.

Data which is forward to the AMCC PCI Controller is configurable. The timestamp, cell header, and cell payload can be passed or discarded on a global basis for qualifying cells. A 52-bit counter that operates at 40 MHz will allow the time stamping of each ATM cell. This generates timestamp ticks at a 25ns resolution. This allows for unique timestamps for each word extracted from the S/UNI device for a period up to 3.57 years before the timestamp counter will roll over. The table below shows the PCI memory layout for an ATM cell with all options enabled.

Byte 3	Byte 2	Byte 1	Byte 0
Lower 20-bits of 52-bit Timestamp			2-bit count value
Upper 32-bits of 52-bit Timestamp			
H4	H3	H2	H1
Payload 4	Payload 3	Payload 2	Payload 1
Payload 8	Payload 7	Payload 6	Payload 5
Payload 12	Payload 11	Payload 10	Payload 9
Payload 16	Payload 15	Payload 14	Payload 13
Payload 20	Payload 19	Payload 18	Payload 17
Payload 24	Payload 23	Payload 22	Payload 21
Payload 28	Payload 27	Payload 26	Payload 25
Payload 32	Payload 31	Payload 30	Payload 29
Payload 36	Payload 35	Payload 34	Payload 33
Payload 40	Payload 39	Payload 38	Payload 37
Payload 44	Payload 43	Payload 42	Payload 41
Payload 48	Payload 47	Payload 46	Payload 45

Table 2: ATM Cell Data Format

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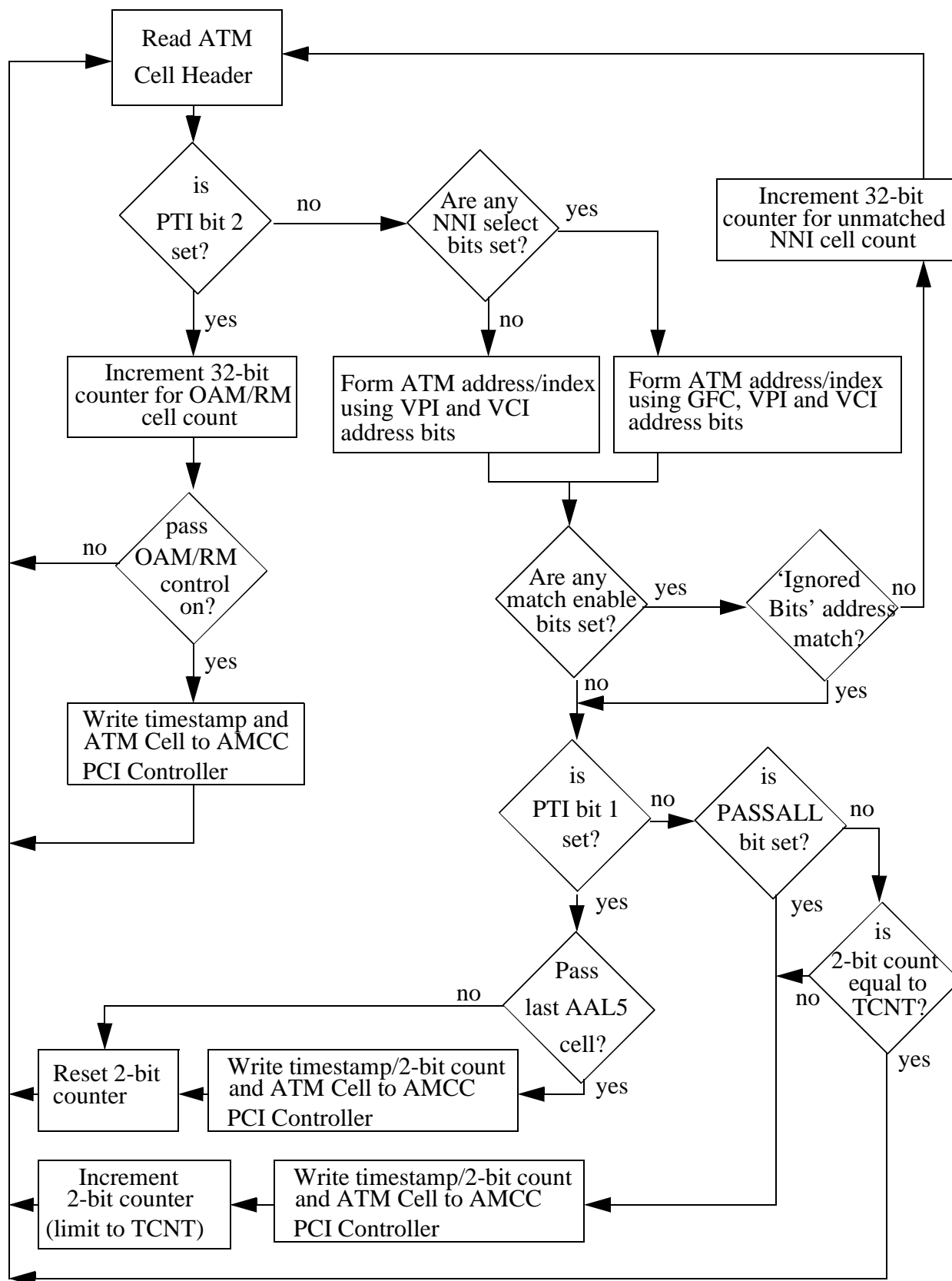
The POINT register map for AAL5 mode is shown in Table 3. All registers are 8-bit bytes mapped into a 32-bit word address space.

Table 3: RXFPGA Registers

Address	R/W	Init	Bit	Contents
0x00				**Control Register I**
	R/W	0	0	**FIFORST#** **0** = Reset external FIFOs **1** = Normal external FIFO operation
	R/W	0	1	**ENCELLS** **0** = Disable S/UNI 622 Receive ATM cell extraction **1** = Enable S/UNI 622 Receive ATM cell extraction
	R/W	0	2	**ENFIFOWR** **0** = Disable writes to external FIFOs **1** = Enable writes to external FIFOs
	R/W	0	3	**ENAMCCWR** **0** = Disable writes from external FIFO to AMCC FIFO **1** = Enable writes from external FIFO to AMCC FIFO
	R/W	0	4	**FIFOLD#** **0** = Enable writes to external FIFO programmable flags. **1** = Normal external FIFO operation
	R/W	0	5	**ENTIMESTAMP** **0** = Timestamp not passed to AMCC Controller **1** = Timestamp passed to AMCC Controller
	R/W	0	6	**ENHEADER** **0** = ATM header not passed to AMCC Controller **1** = ATM header passed to AMCC Controller
	R/W	0	7	**ENPAYLOAD** **0** = ATM payload not passed to AMCC Controller **1** = ATM payload passed to AMCC Controller
0x04				**Status Register I** **External FIFO Status Flags**
	R		0	External FIFO Empty Flag (active high)
	R		1	External FIFO programmable Almost Empty Flag (active high)
	R		2	External FIFO programmable Almost Full Flag (active high)
	R		3	External FIFO Full Flag (active high)
	LR		4	Latched External FIFO Almost Full Flag (active high, reset when read)
	LR		5	Latched External FIFO Full Flag (active high, reset when read)
	LR		6	Latched Receive ATM data parity error (active high, reset when read)

Table 3: RXFPGA Registers

Address	R/W	Init	Bit	Contents
0x08	R/W	0x00	7-0	**External FIFO Programmable Flag Data** Data written to this register will written to the external FIFO programmable flags (via a single write cycle) provided that the FIFOLD# control is active.
0x0C				**Control Register II**
	R/W	000	2-0	**NNI Select bits** These three bits contain a count of the number of extended VPI bits to replace upper VCI bits. 000 = no extended VPI bits 001 = VPI bit 8 replaces VCI bit 15 010 = same as 001 setting + VPI bit 9 replaces VCI bit 14 011 = same as 010 setting + VPI bit 10 replaces VCI bit 13 100 = same as 011 setting + VPI bit 11 replaces VCI bit 12 101 - 111 = same as 000 setting (no extended VPI bits)
	R/W	0	3	**PASSALL** **0** = Forward cell data according to TCNT setting **1** = Forward all AAL5 ATM cells, disregard TCNT restriction
	R/W	0	4	**0** = Discard OAM/RM cells **1** = Pass all OAM/RM cells to AMCC PCI Controller
	R/W	0	5	**0** = Pass beginning AAL5 ATM cells only (up to TCNT). **1** = Pass last AAL5 cell (as indicated by PTI bit 1 being set) to AMCC PCI Controller.
	R/W	00	7-6	**TCNT** These two bits set the number of beginning AAL5 ATM cells to pass to the AMCC PCI Controller (0x0 = no cells, 0x1 = one cell, 0x2 = two cells, 0x3 = three cells).
0x10				**Match Register**
	R/W	0000	3-0	**Match Value bits** These bits are used to compare ignored bits (extended VPI or lower VCI address bits)
	R/W	0000	7-4	**Enable Match Bits** These bits will enable matching of ignored address bits against the Match Value bits
0x14	R/W	0x00	7-0	**SRAM Address A7 - A0** This register contains address information to allow PCI access to POINT's SRAM memory
0x18	R/W	0x00	7-0	**SRAM Address A15 - A8** This register contains address information to allow PCI access to POINT's SRAM memory

Table 3: RXFPGA Registers

Address	R/W	Init	Bit	Contents
0x1C	R/W	0000	3-0	**SRAM Address A19 - A16** This register contains address information to allow PCI access to POINT's SRAM memory.
			5-4	**Reserved**
	R/W	0	6	**SRAM R#/W Control** **0** = When SRAM Cycle bit is set, read SRAM and place data into SRAM Data Registers 0 thru 3. **1** = When SRAM Cycle bit is set, write SRAM with data stored in SRAM Data Registers 0 thru 3.
	R/W	0	7	**SRAM Cycle** Setting this bit to 1 will cause a single read or write cycle to occur to the SRAM memory using the address set in the SRAM address registers. This bit will reset to zero when the SRAM access is complete.
0x20	R/W	0x00	7-0	**SRAM Data Register 0 (D7 - D0)** This register contains either data read from or data to write to POINT's SRAM memory.
0x24	R/W	0x00	7-0	**SRAM Data Register 1 (D15 - D8)** This register contains either data read from or data to write to POINT's SRAM memory.
0x28	R/W	0x00	7-0	**SRAM Data Register 2 (D23 - D16)** This register contains either data read from or data to write to POINT's SRAM memory.
0x2C	R/W	0x00	7-0	**SRAM Data Register 3 (D31 - D24)** This register contains either data read from or data to write to POINT's SRAM memory.
0x30	R/W	0	0	**Cell Count Transfer/Reset** Setting this bit to 1 will cause the OAM/RM Cell Counter and the Unmatched NNI Cell Counter to transfer the current count values to their respective counter read registers and to reset the counters back to zero. This control bit will reset to zero when the transfer and reset has completed.
			7-1	**Reserved.**
0x34	R	0x00	7-0	**OAM/RM Cell Counter Read Register (Q7 - Q0)** This register contains the least significant byte of the OAM/RM cell counter.
0x38	R	0x00	7-0	**OAM/RM Cell Counter Read Register (Q15 - Q8)** This register contains the second least significant byte of the OAM/RM cell counter.
0x3C	R	0x00	7-0	**OAM/RM Cell Counter Read Register (Q23 - Q16)** This register contains the second most significant byte of the OAM/RM cell counter.
0x40	R	0x00	7-0	**OAM/RM Cell Counter Read Register (Q31 - Q24)** This register contains the most significant byte of the OAM/RM cell counter.
0x44	R	0x00	7-0	**Unmatched NNI Cell Counter Read Register (Q7 - Q0)** This register contains the least significant byte of the unmatched NNI cell counter.

Table 3: RXFPGA Registers

Address	R/W	Init	Bit	Contents
0x48	R	0x00	7-0	**Unmatched NNI Cell Counter Read Register (Q15 - Q8)** This register contains the second least significant byte of the unmatched NNI cell counter.
0x4C	R	0x00	7-0	**Unmatched NNI Cell Counter Read Register (Q23 - Q16)** This register contains the second most significant byte of the unmatched NNI cell counter.
0x50	R	0x00	7-0	**Unmatched NNI Cell Counter Read Register (Q31 - Q24)** This register contains the most significant byte of the unmatched NNI cell counter.
0x78	R/W	0x00	7-0	**Diagnostic Register** This register is a generic read/write register for diagnostic purposes.
0x7C	R	0	0	**XOR Address Bit** This bit contains the exclusive OR of address bits A2 - A9 (PTA0 - PTA7) from the PREVIOUS read or write access to the FPGA and is used for diagnostic purposes.