ESS Technology, Inc.

Maestro-2E™ PCI Audio Accelerator Data Sheet

DESCRIPTION

The Maestro-2E™ PCI audio accelerator, a high-performance 500-MIPS-equivalent PCI audio processor, uses the high-bandwidth PCI bus and an AC'97 CODEC to deliver advanced PC audio features. These features include HRTF 3-D positional audio, high-quality 64-channel wavetable music synthesis with downloadable wavetable samples, and DVD AC-3 5.1-to-2 speaker virtualization.

The Maestro-2E implements multi-stream DirectSound and DirectSound3D acceleration and Windows 95 and Windows 98 stream acceleration with digital mixing and sample rate conversion. The Maestro-2E maintains full DOS legacy audio compatibility over a standard PCI 2.1 bus. The Maestro-2E is designed for high-performance consumer multimedia PC, notebook PC, and add-in card applications.

The Maestro-2E, based on a dual-engine, 64-channel, pipelined Wave Processor and a programmable audio signal processor, provides simultaneous support for multiple audio streams of different types. Its core architecture is designed to handle complex signal processing tasks with a bus-mastering PCI interface and built-in dedicated DMA engine supporting a DSP core. The support functions ensure efficient transfer of audio data streams to and from system memory buffers, providing a system solution with maximum performance and minimal host CPU loading. The architecture enables implementation of communications over the Internet from multiple sources.

The Maestro-2E has a variety of audio interfaces. It has two 20-bit AC'97 CODEC interfaces that can be enabled simultaneously for notebook docking implementation. The secondary AC'97 CODEC interface can be programmed to handle multiple serial CODEC interfaces which, together with the primary AC'97 CODEC, can provide full-featured AC-3 speaker outputs. The Maestro-2E also supports a consumer IEC958 S/PDIF output that provides high-quality digital audio and MIDI.

The Maestro-2E, which operates at 3.3 volts, has several special features for notebook operation. It is compliant with the Advanced Power Management (APM) 1.2, Advanced Configuration and Power Interface (ACPI) 1.0, and PCI Power Management Interface (PPMI) 1.0. It has multiple power-saving modes (D0, D1, D2, and D3) for power-efficiency when the audio system is both active and idle. It provides a high-quality docking solution that is backward compatible to the ES978 docking station interface, and also supports an AC-link based digital docking solution with its secondary 20-bit AC-link. CLKRUN# pin support can be used to stop the PCI interface clock. This helps achieve the lowest power consumption in $D3_{hot}$ mode.

The Maestro-2E supports full DOS game compatibility for both PC motherboard and add-in card solutions through three hardware implementations: PC/PCI, Distributed DMA (DDMA), and Transparent DMA (TDMA). While PC/PCI and DDMA are industry-standard protocols for legacy support, ESS' TDMA technology implements DOS game compatibility over the standard PCI 2.1 bus without additional sideband signals.

The Maestro-2E PCI audio accelerator is pin-to-pin compatible to the Maestro-2, and is available in an industry-standard 100-pin Thin Quad Flat Package (TQFP).

FEATURES

High-Performance PCI Audio Acceleration

- 500-MIPS-equivalent dual-engine PCI audio accelerator
- 64-Channel wavetable synthesis
- HRTF 3-D positional audio acceleration
- Multi-Stream DirectSound and DirectSound3D acceleration
- Hardware acceleration for DirectMusic, ActiveMovie, and DirectInput API
- DVD AC-3 speaker virtualization
- Enhanced effects (reverb, chorus, flange, treble, bass, and 3D stereo expander)
- Advanced platform for interactive 3-D gaming, DVD movie playback, and Internet communications

Legacy DOS Game Support

- Full DOS game compatibility through three hardware implementations: PC/PCI, DDMA, and TDMA
- TDMA needs no sideband signals, full DOS game compatibility achieved in standard PCI 2.1 bus
- Serial IRQ support

Complete Audio Solution for Notebook PCs

- Compliance with APM 1.2, ACPI 1.0, and PPMI 1.0
- Compliance with Intel's "Mobile Power Guideline"
- 3.3 volt operation with multiple power-saving modes

- Digital docking interface through AC-link
- Docking interface backward compatible with ES978 Mixer
- CLKRUN# pin support

Flexible Audio I/O Interface

- 20-Bit AC'97 ext. 1.03/2.00 CODEC interface
- Multiple CODEC interface to 6 speaker outputs
- I²S Zoomed Video interface
- External DSP serial interface
- 2-Button hardware master volume control

Digital Ready

- S/PDIF output contains Digital Audio and MIDI
- Windows 98 WDM acceleration
- USB/1394 Digital Ready

Package

- 100-Pin TQFP

CONTENTS

FIGURES

TABLES

MAESTRO-2E BLOCK DIAGRAMS

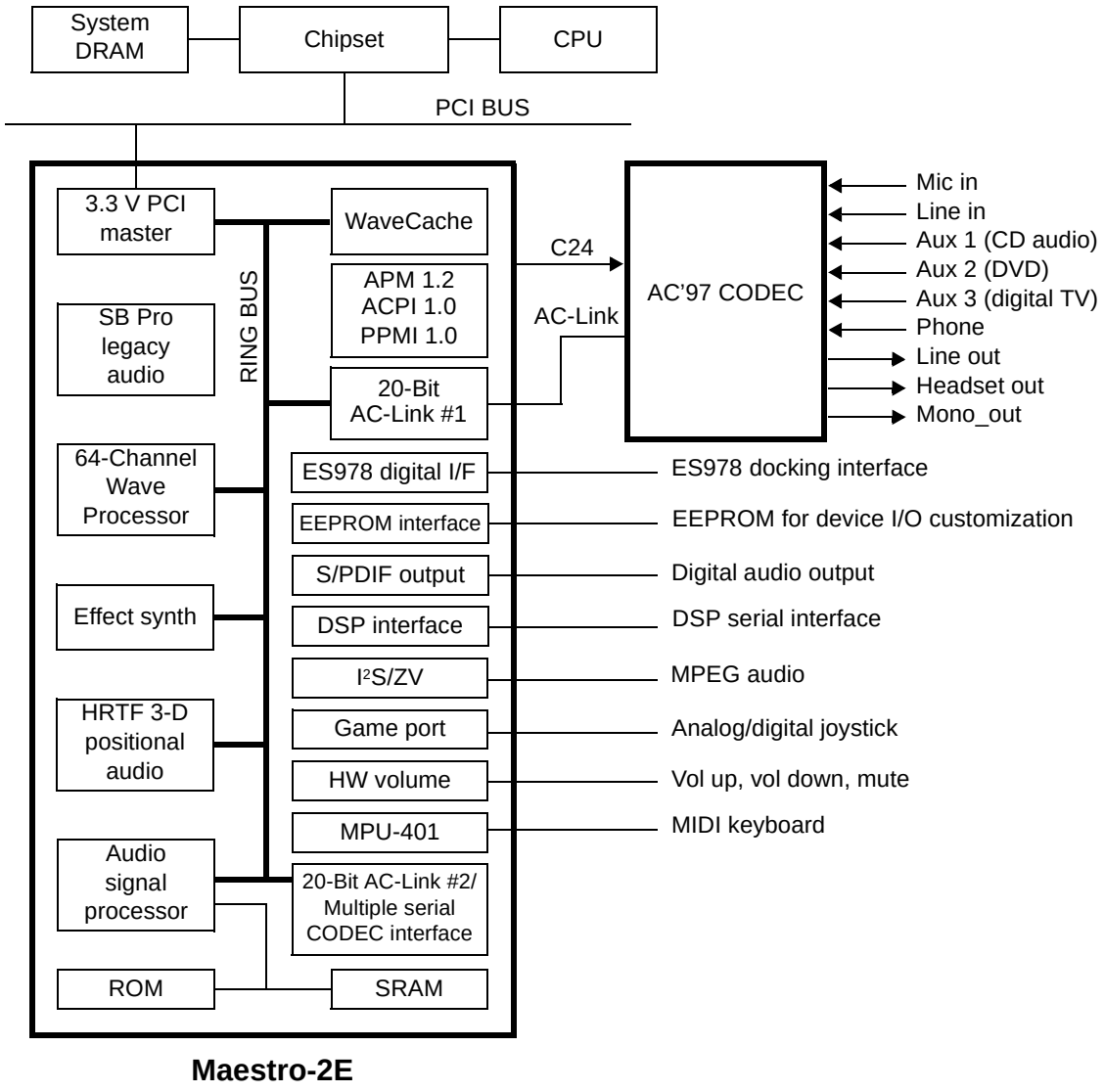


Figure 1 Maestro-2E Block Diagram

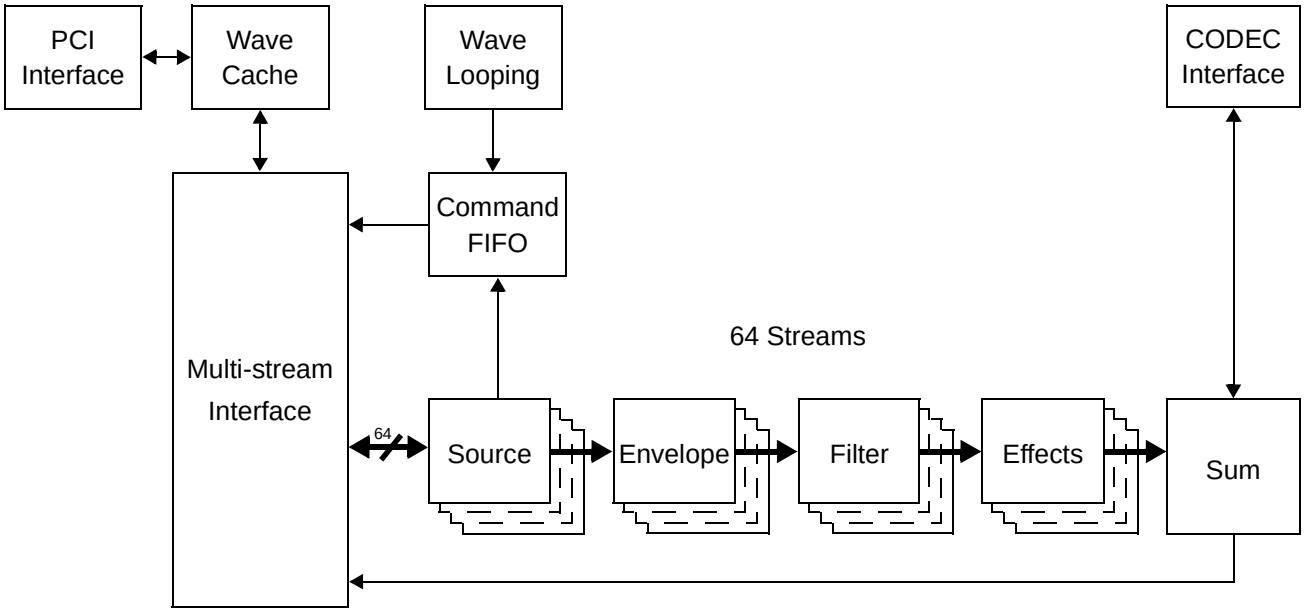


Figure 2 Wave Processor Portion

DOCKING APPLICATIONS

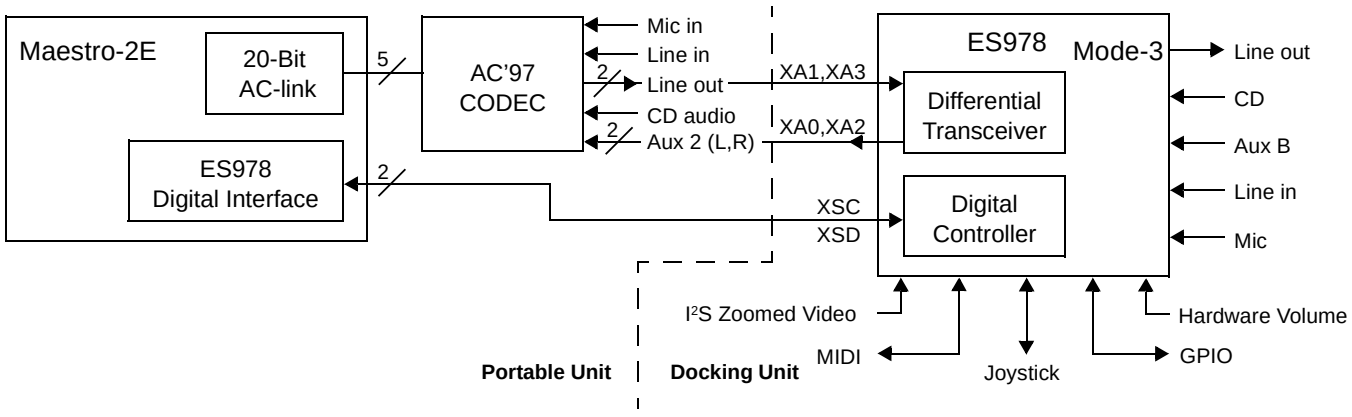


Figure 3 Docking Interface – Backward Compatible to the ES978

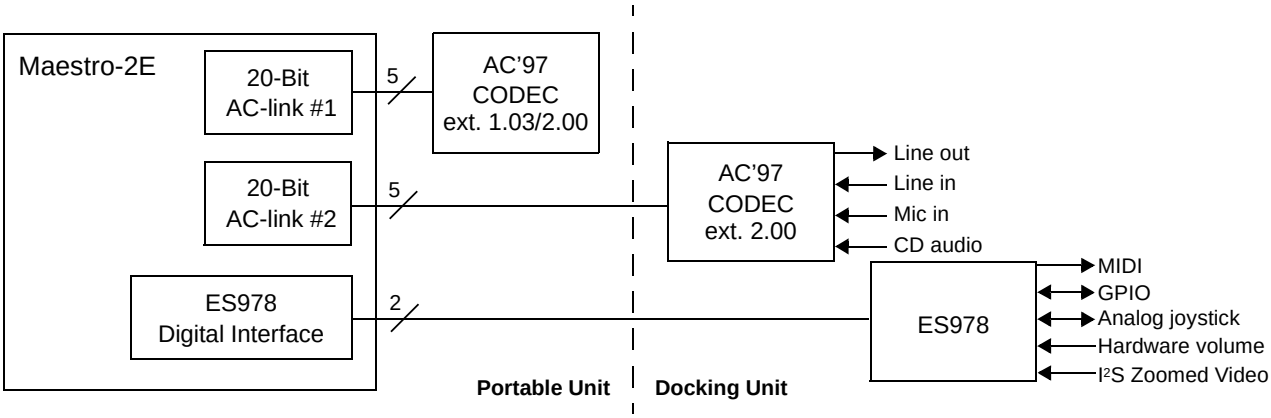


Figure 4 Digital Docking Interface

PINOUT

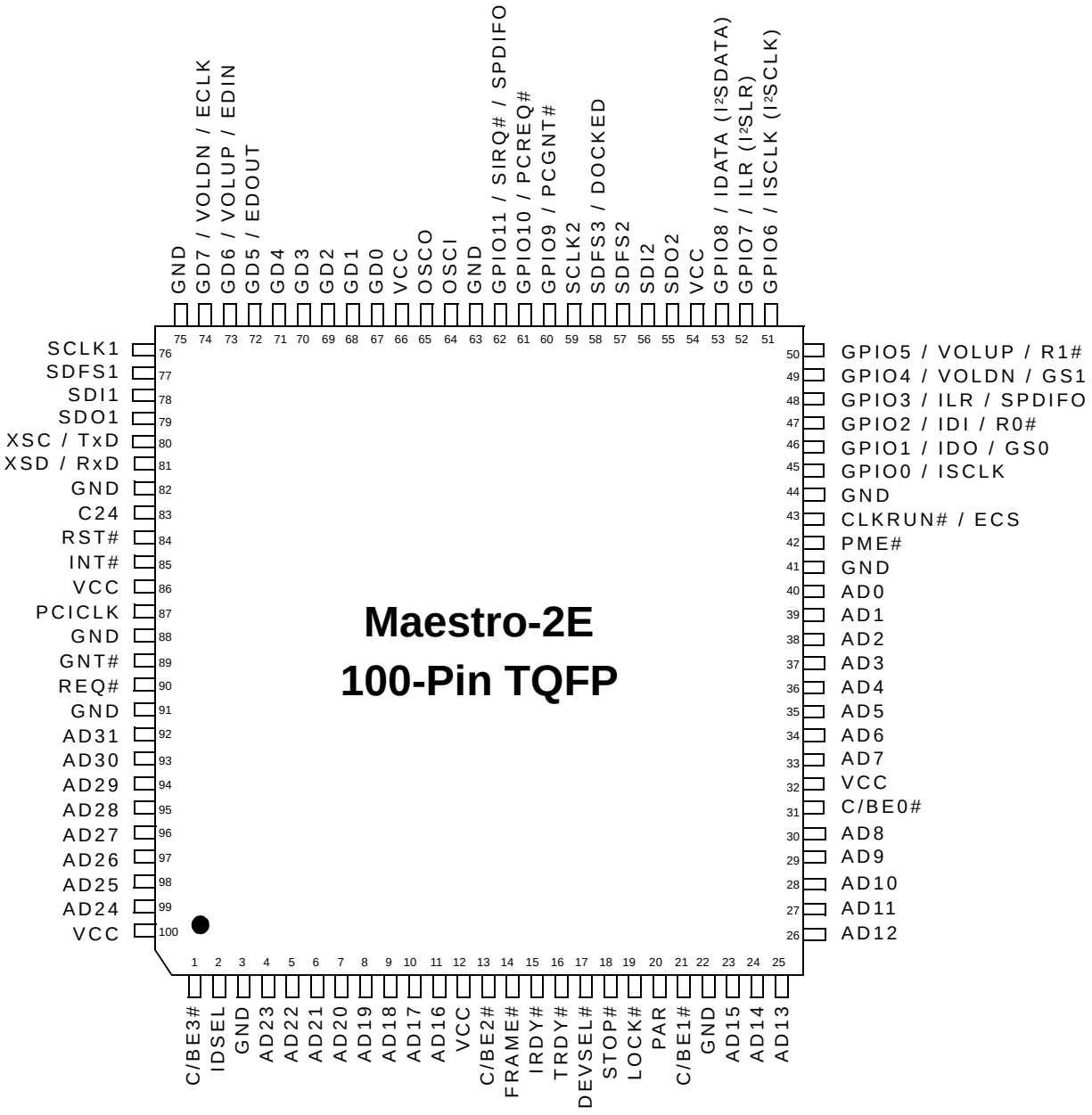


Figure 5 Maestro-2E Pinout

PIN DESCRIPTION

Name	Number	I/O	Definition	
C/BE[3:0]#	1,13,21,31	I/O	Multiplexed command/byte enable. These pins indicate cycle type during the address phase of a transaction. They indicate active-low byte enable information for the current data phase during the data phases of a transaction. These pins are inputs during slave operation and outputs during bus mastering operation.	
IDSEL	2	I	ID select, active-high. This pin is used as a chip select during PCI configuration read and write cycles.	
AD[31:0]	92:99,4:11, 23:30,33:40	I/O	Multiplexed address and data lines.	
FRAME#	14	I/O	Cycle frame, active-low. The current PCI bus master drives this pin to indicate the beginning and duration of a transaction.	
IRDY#	15	I/O	Initiator ready, active-low. The current PCI bus master drives this pin to indicate that as the initiator it is ready to transmit or receive data (and complete the current data phase).	
TRDY#	16	I/O	Target ready, active-low. The current PCI bus master drives this pin to indicate that as the target device it is ready to transmit or receive data (and complete the current data phase).	
DEVSEL#	17	I/O	Device select, active-low. The PCI bus target device drives this pin to indicate that it has decoded the address of the current transaction as its own chip select range.	
STOP#	18	I/O	Stop transaction, active-low. The current PCI bus target drives this pin active to indicate a request to the master to stop the current transaction.	
LOCK#	19	I/O	Lock.	
PAR	20	I/O	Parity, active-high. This pin indicates even parity across AD[31:0] and C/BE[3:0]# for both address and data phases. The signal is delayed one PCI clock from either the address or data phase for which parity is generated.	
PME#	42	O	Power management enable interrupt output to wake up the system.	
CLKRUN#	43	I/O	Dual-purpose pin. CLKRUN# is an input for clock status and an output to start/speed-up clock.	
ECS		O	ECS# is the EEPROM chip select. ECS is active during power-on reset; turned off after reset.	
GPIO0	45	I/O	Dual-purpose pin. GPIO0 is general purpose input/output 0. Selected by Maestro2E_Base+68h[11:0].	
ISCLK		I	ISCLK is the serial shift clock for the DSP serial interface. Selected by setting PCI 52h[4] = 1 and Maestro2E_Base+36h[15] = 1.	
GPIO1	46	I/O	Multi-purpose pin. GPIO1 is general purpose input/output 1. Selected by Maestro2E_Base+68h[11:0].	Strap pin: 1 = TDMA mode for 440LX chipset (default). 0 = PC/PCI mode for 440LX chipset.
IDO		O	IDO is the serial data output for the DSP serial interface. Selected by setting PCI 52h[4] = 1 and Maestro2E_Base+36h[15] = 1.	
GS0		O	GS0 is PCI bus grant select 0. Selected by setting PCI 58h[0] = 1.	
GPIO2	47	I/O	Multi-purpose pin. GPIO2 is general purpose input/output 2. Selected by Maestro2E_Base+68h[11:0].	
IDI		I	IDI is the serial data input for the DSP serial interface. Selected by setting PCI 52h[4] = 1 and Maestro2E_Base+36h[15] = 1.	
R0#		I	R0# is PCI bus request 0. Selected by setting PCI 58h[0] = 1.	
GPIO3	48	I/O	Multi-purpose pin. GPIO3 is general purpose input/output 3. Selected by Maestro2E_Base+68h[11:0].	
ILR		I	ILR is the frame sync signal for the DSP serial interface. Selected by setting PCI 52h[4] = 1 and Maestro2E_Base+36h[15] = 1.	
SPDIFO		O	SPDIFO is the S/PDIF output. Selected by setting PCI 53h[0] = 1 and PCI 58h[1] = 0. Alternatively, the SPDIFO at pin 62 may be used. SPDIFO at pin 48 is the default.	

Name	Number	I/O	Definition	
GPIO4	49	I/O	Multi-purpose pin. GPIO4 is general purpose input/output 4. Selected by Maestro2E_Base+68h[11:0].	Strap pin: 1 = Subsystem ID[0] = 0. 0 = Subsystem ID[0] =1.
VOLDN		I	VOLDN is a volume decrease input. Selected by setting PCI 52h[7:5] to 1x0. Alternatively, the VOLUP/VOLDN pair at pins 73 and 74 may be used.	
GS1		O	GS1 is PCI bus grant select 1. Selected by setting PCI 58h[0] = 1.	
GPIO5	50	I/O	Multi-purpose pin. GPIO5 is general purpose input/output 5. Selected by Maestro2E_Base+68h[11:0].	
VOLUP		I	VOLUP is a volume increase input. Selected by setting PCI 52h[7:5] to 1x0. Alternatively, the VOLUP/VOLDN pair at pins 73 and 74 may be used.	
R1#		I	R1# is PCI bus request 1. Selected by setting PCI 58h[0] = 1.	
GPIO6	51	I/O	Dual-purpose pin. GPIO6 is general purpose input/output 6. Selected by Maestro2E_Base+68h[11:0].	
ISCLK (I^2SCLK)		I	ISCLK (I^2SCLK) is the I^2S serial clock. Selected by setting Maestro2E_Base+36h[15] = 1.	
GPIO7	52	I/O	Dual-purpose pin. GPIO7 is general purpose input/output 7. Selected by Maestro2E_Base+68h[11:0].	
ILR (I^2SLR)		I	ILR (I^2SLR) is the I^2S frame sync. Selected by setting Maestro2E_Base+36h[15] = 1.	
GPIO8	53	I/O	Dual-purpose pin. GPIO8 is general purpose input/output 8. Selected by Maestro2E_Base+68h[11:0].	
IDATA (I^2SDATA)		I	IDATA (I^2SDATA) is the I^2S data input pin. Selected by setting Maestro2E_Base+36h[15] = 1.	
SDO2	55	I/O	Serial data out.	
SDI2	56	I	Serial data in.	
SDFS2	57	O	Serial data frame sync. Strap pin in combination with strap pin 77. See the description for pin 77.	
SDFS3	58	O	Dual-purpose pin. SDFS3 is the serial data frame sync.	
DOCKED		I	DOCKED, when active-high, indicates that the unit is docked to an AC'97 CODEC with docking station support. Internal 2.2k pull-down to digital ground.	
SCLK2	59	I/O	Serial data clock. Output pin when the multi-CODEC interface is used. Input pin when the AC-link #2 interface is used.	
GPIO9	60	I/O	Dual-purpose pin. GPIO9 is general purpose input/output 9. Selected by Maestro2E_Base+68h[11:0].	
PCGNT#		I	PCGNT# is the PC/PCI grant input. Selected by setting PCI 50h[10:8] = 010.	
GPIO10	61	I/O	Dual-purpose pin. GPIO10 is general purpose input/output 10. Selected by Maestro2E_Base+68h[11:0].	
PCREQ#		O	PCREQ# is the PC/PCI request output. Selected by setting PCI 50h[10:8] = 010.	
GPIO11	62	I/O	Multi-purpose pin. GPIO11 is general purpose input/output 11. Selected by Maestro2E_Base+68h[11:0].	
SIRQ#		I/O	SIRQ# is the serial interrupt request. Selected by setting PCI 40h[14] = 1.	
SPDIFO		O	SPDIFO is the S/PDIF output. Selected by setting PCI 53h[0] = 1 and PCI 58h[1] = 1. Alternatively, the SPDIFO at pin 48 may be used. SPDIFO at pin 48 is the default.	
OSCI	64	I	49.152 MHz crystal input. Refer to the Maestro-2 reference design for an update.	
OSCO	65	O	49.152 MHz crystal output. Refer to the Maestro-2 reference design for an update.	
GD[3:0]	70:67	I/O	Game port data. Joystick timer.	
GD4	71	I	Game port data. Joystick switch.	

Name	Number	I/O	Definition
GD5	72	I	Dual-purpose pin. GD5 is a game port data input pin.
EDOUT		O	EDOUT is EEPROM data output. EDOUT is active during power-on reset; turned off after reset.
GD6	73	I	Dual-purpose pin. GD6 is a game port data input pin.
VOLUP		I	VOLUP is a volume increase input. Selected by setting PCI 52h[7:5] = 1x1. Alternatively, the VOLDN/VOLUP pair at pins 49 and 50 may be used.
EDIN		I	EDIN is EEPROM data input. EDIN is active during power-on reset; turned off after reset.
GD7	74	I	Dual-purpose pin. GD7 is a game port data input pin.
VOLDN		I	VOLDN is a volume decrease input. Selected by setting PCI 52h[7:5] = 1x1. Alternatively, the VOLDN/VOLUP pair at pins 49 and 50 may be used.
ECLK		O	ECLK is the EEPROM clock output. ECLK is active during power-on reset; turned off after reset.
SCLK1	76	I	Serial clock. In AC'97 configuration, this pin is an input which drives the timing for the AC'97 interface.
SDFS1	77	O	Serial data frame sync. In AC'97 configurations, this strap pin is an output which indicates the framing for the AC'97 link with pin 57. **Pin 57** / **Pin 77** / **Option** 0 / 0 / Reserved. 0 / 1 / Reserved. 1 / 0 / Multi-CODEC pinout at pins 59:55. 1 / 1 / AC-Link#2 pinout at pins 57:55, and 59.
SDI1	78	I	Serial audio data input.
SDO1	79	O	Serial audio data out.
TxD	80	O	Dual-purpose pin. TxD is MIDI transmit data.
XSC		O	XSC is the ES978 Expansion Audio Mixer serial clock. Selected by setting PCI 58h[2] = 1 while the DOCKED pin is high.
RxD	81	I	Dual-purpose pin. RxD is MIDI receive data.
XSD		I/O	XSD is the ES978 Expansion Audio Mixer serial data input/output. Selected by setting PCI 58h[2] = 1 while the DOCKED pin is high.
C24	83	O	24.576 MHz clock output. For CODEC clock source.
RST#	84	I	Reset.
INT#	85	O	Interrupt request, active-low. This pin is the level triggered interrupt pin dedicated to servicing internal device interrupt sources.
PCICLK	87	I	PCI bus clock. This clock times all PCI transactions. All PCI synchronous signals are generated and sampled relative to the rising edge of this clock.
GNT#	89	I	Bus master grant, active-low. The system arbiter drives this pin to indicate to the device that access to the PCI bus has been granted.
REQ#	90	O	Bus master request, active-low tri-state output. This pin indicates to the system arbiter that this device is requesting access to the PCI bus. This pin must be tri-stated when RST# is active.
VCC	12,32,54, 66,86,100	Pwr	+3.3 volts.
GND	3,22,41,44, 63,75,88,91	Pwr	Ground.

STRAP SELECTED OPTION

Pin Name	Pin Number	Default State at Reset	Condition	Description
SDFS2	57	Pull-up	See Description	In AC'97 configurations, this strap pin is an output which indicates the framing for the AC'97 link with pin 57. **Pin 57 / Pin 77 / Option** 0 / 0 / Reserved. 0 / 1 / Reserved. 1 / 0 / Multi-CODEC pinout at pins 59:55. 1 / 1 / AC-Link#2 pinout at pins 57:55, and 59.
SDFS1	77	Pull-up	See Description	See description of pin 57.
GPIO1	46	Pull-up	Low	PC/PCI system configuration is detected.
			High	No PC/PCI system configuration is detected. TDMA mode for 440LX chipset.
GPIO4	49	Pull-up	Low	Bit 0 of PCI Configuration register 2Eh =1.
			High	Bit 0 of PCI Configuration register 2Eh =0.

MULTI-FUNCTION PIN ASSIGNMENT

Function	Pin Names	Pin Numbers	Selection Settings
DSP Serial Interface	ISCLK,IDO,IDI,ILR	48:45	PCI 52h[4] = 1 and Maestro2E_Base+36h[15]=1
EEPROM Interface	ECS#,EDOUT, EDIN,ECLK	43,74:72	Active during power-on reset. Turned off after reset.
ES978 Mixer Expansion Interface	XSC,XSD	81:80	PCI 58h[2] = 1 and DOCKED pin high
General-Purpose Interface	GPIO[11:0]	62:60,53:45	Maestro2E_Base+68h[11:0]
Hardware Volume Control	VOLUP,VOLDN	50,49	PCI 52h[7:5] = 1x0
	VOLUP,VOLDN	73,74	PCI 52h[7:5] = 1x1
I^2S Interface	ISCLK,ILR,IDATA	53:51	Maestro2E_Base+36h[15] = 1
Legacy Audio Interface	PCGNT#,PCREQ#	61:60	PCI 50h [10:8] = 010
	SIRQ#	62	PCI 40h[14] = 1
Multiple PCI Master Interface	R[1:0]#,GS[1:0]	47,50,46,49	PCI 58h[0] = 1
Secondary AC'97 Interface (AC'97 Extension 2.00)	SCLK2,SDFS2, SDI2,SDO2	59, 57:55	Strap pin 57 high; strap pin 77 high
Serial CODEC Interface	SCLK2,SDFS3, SDFS2,SDI2,SDO2	59:55	Strap pin 57 high; strap pin 77 low
S/PDIF Output	SPDIFO	48 (default)	PCI 53h[0] = 1 and PCI 58[1] = 0
		62	PCI 53h[0] = 1 and PCI 58h[1] = 1

FUNCTIONAL PIN GROUPING

Function	Pins	Pin Number
ACPI Pin	PME#	42
CODEC #1 Interface	SCLK1	76
	SDFS1	77
	SDI1	78
	SDO1	79
Clocks	OSCI	64
	OSCO	65
	C24	83
Docking Station Interface Pin	DOCKED *	58
DSP Serial Interface	ISCLK *	45
	IDO *	46
	IDI *	47
	ILR *	48
EEPROM Interface Pins	ECS *	43
	ECLK *	74
	EDOUT *	72
	EDIN *	73
ES978 Mixer Expansion Interface Pins	XSC *	80
	XSD *	81
Game Port Interface	GD[3:0]	70:67
	GD4	71
	GD5 *	72
	GD6 *	73
	GD7 *	74
General-Purpose I/O Pins	GPIO0 *	45
	GPIO1 *	46
	GPIO2 *	47
	GPIO3 *	48
	GPIO4 *	49
	GPIO5 *	50
	GPIO6 *	51
	GPIO7 *	52
	GPIO8 *	53
	GPIO9 *	60
	GPIO10 *	61
	GPIO11 *	62
Hardware Volume Control Pins	VOLDN *	49,74
	VOLUP *	50,73

Function	Pins	Pin Number
I²S Interface	ISCLK (I²SCLK) *	51
	ILR (I²SLR) *	52
	IDATA (I²SDATA) *	53
Legacy Audio Interface	PCGNT# *	60
	PCREQ# *	61
	SIRQ# *	62
MPU-401 Interface	TxD *	80
	RxD *	81
Multiple PCI Master Interface	R0# *	47
	R1# *	50
	GS0 *	46
	GS1 *	49
PCI Bus Pins	IDSEL	2
	AD[31:0]	92:99,4:11, 23:30,33:40
	C/BE[3:0]#	1,13,21,31
	FRAME#	14
	IRDY#	15
	TRDY#	16
	DEVSEL#	17
	STOP#	18
	LOCK#	19
	PAR	20
	CLKRUN#	43
	RST#	84
	INT#	85
	PCICLK	87
	GNT#	89
	REQ#	90
Serial CODEC Interface / Secondary AC'97 Interface	SDO2	55
	SDI2	56
	SDFS2	57
	SDFS3 *	58
	SCLK2	59
S/PDIF Output	SPDIFO *	48, 62
Power Pins	VCC	100,86,66, 54,32,12
	GND	91,88,75,63, 44,41,22,3

* These pins share more than one function.

POWER MANAGEMENT

The Maestro-2E is a high-performance device with low power consumption. Besides the low-power CMOS technology used to process the Maestro-2E, various features are designed into the device to provide benefits from popular power-saving techniques. These features and techniques are discussed in this section.

CLKRUN Protocol

The PCI CLKRUN feature is one of the primary methods of power management on the PCI bus interface of the Maestro-2E for the notebook computer. Since some chipsets do not implement CLKRUN, this is not always available to the system designer, and alternate power-saving features are provided.

PCI Power Management Interface (PPMI)

The PCI Power Management Interface (PPMI) specification establishes the infrastructure required to let the operating system control the power of PCI functions. This is done by defining a standard PCI interface and operations to manage the power of PCI functions on the bus. The PCI functions can be assigned one of five power management states that result in varying levels of power savings.

The five power-management states of PCI functions are:

- D0 – full power
- D1 and D2 – intermediate states
- D3 hot – off state; power supply is on
- D3 cold – off state; power supply is off

For the operating system to manage the device power states on the PCI bus, the PCI function should support four power-management operations:

– capabilities reporting
– power status reporting
– setting the power state
– system wake-up

The operating system identifies the capabilities of the PCI function by traversing the new capabilities list. The presence of new capabilities is indicated by setting bit [4] in the PCI Status register and providing access through a capabilities pointer to a capabilities list.

The capabilities pointer provides access to the first item in the linked list of capabilities. For the Maestro-2E, the capabilities pointer is mapped to an offset, C0h, indicated in the PCI Configuration register at 34h. The first byte of each capability register block is required to be a unique ID of the capability. PCI power management has been assigned an ID of 01h. The next byte is a pointer to the next pointer item in the list of capabilities. There are no more items in the list, so the next item pointer is set to zero. The registers following the next item pointer are specific to that function's capability. The PPMI capability implements the register block outlined in Table 1.

The Power-Management Capabilities register (PCI Configuration register C2h in the Maestro-2E) is a static read-only register that provides information on the capabilities of the functions related to power-management. The Power-Management Control/Status register enables control of power-management states and enables and monitors power-management events. The Data register is an optional register that displays state-dependent power measurements such as power consumed or heat dissipation.

Table 1 Power-Management Registers

Register Name				**Offset**
Power-Management capabilities		Next-Item pointer	Capability ID	0
Data	PMCSR bridge support extensions	Power-Management control status (CSR)		4

ACPI Transition Diagram

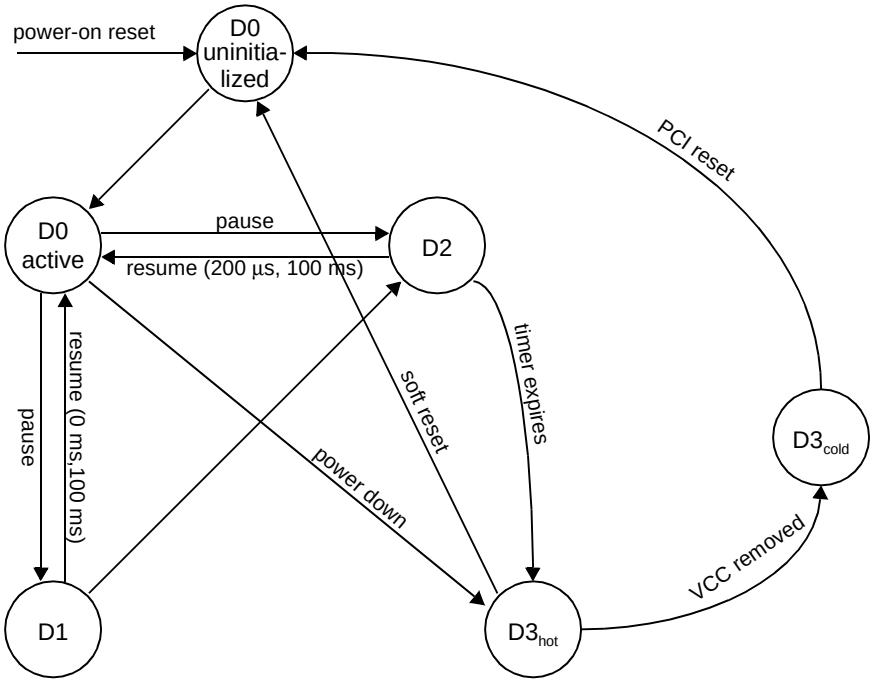


Figure 6 ACPI Transition Diagram

DISABLING MAESTRO-2E AUDIO

To disable Maestro-2E audio in both notebook and motherboard implementations:

1. Set PCI 04h[2:0] = 000.

   This disables Maestro-2E response to all inputs and outputs and Bus Master cycles.

2. Set PCI 40h[7] = 1.

   This disables Maestro-2E response to all legacy audio functions.

PCI CONFIGURATION REGISTERS

Register Summary

Table 2 PCI Configuration Registers Summary

2F	20	1F	0	**Offset**
Device ID		Vendor ID		00h
Device capability		Status	Command	04h
Base class code	Sub-class code	Programming interface identifier	Revision ID	08h
BIST capability	Header type	Latency timer	Cache line size	0Ch
Reserved		Maestro-2E I/O space base address		10h
Reserved				14h
Reserved				18h
Reserved				1Ch
Reserved				20h
Reserved				24h
Reserved				28h
Subsystem ID (R/W protected)		Subsystem vendor ID (R/W protected)		2Ch
Reserved				30h
Reserved			Capability pointer	34h
Reserved				38h
Max_Lat	Min_Gnt	Interrupt pin	Interrupt line	3Ch
Reserved		Legacy audio control		40h
Reserved		Reserved		44h
Reserved		Reserved		48h
Reserved		Reserved		4Ch
Maestro-2E configuration B		Maestro-2E configuration A		50h
ACPI control B		ACPI control A		54h
Reserved		User Configuration A		58h
Reserved		Reserved		5Ch
Reserved		Distributed DMA		60h
Power-Management capabilities		Next-Item pointer	Capability ID	C0h
Reserved		Power-Management control/status		C4h

All reserved locations are read-only with a default value of zero.

Register Descriptions

Vendor ID (00h, 01h, R)

Vendor ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	Vendor ID	Identifies ESS as the manufacturer of this device. The ID for ESS is 125Dh.

Device ID (02h, 03h, R)

Device ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	Device ID	Identifies Maestro-2E as this device. This ID 1978h is assigned by ESS Technology, Inc.

Command (04h, R/W)

0	0	0	0	0	BM	MS	IO
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:3	–	Read-only. Returns 0 when read.
2	BM	Bus Master enable/disable. 1 = Enable bus master. 0 = Not bus master.
1	MS	Memory Space access enable/disable. Read-only. Set to 0. 1 = Enable memory space access. 0 = Disable memory space access.
0	IO	I/O Space access enable/disable. 1 = Enable I/O space access. 0 = Disable I/O space access.

Status (05h, R)

0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	–	Read-only. Returns 00h when read.

Device Capability (06h, 07h, R)

Device capability															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	DC	The device capability code is 0290h.

9Revision ID (08h, R)

Revision ID							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	Revision ID	Identifies the revision of this device. The ID 00h is assigned by ESS Technology, Inc.

Programming Interface Identifier (09h, R)

Programming interface identifier							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	PII	Identifies the programming interface of this device. The ID 00h indicates a default interface.

Sub-Class Code (0Ah, R)

Sub-Class code							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	SCC	Identifies the type of sub-class of this device. The ID 01h indicates an audio device.

Base Class Code (0Bh, R)

Base class code							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	BCC	Identifies the type of base class of this device. The ID 04h indicates a multimedia device.

Cache Line Size (0Ch, R/W)

Cache line size							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	CLS	Identifies the cache line size of this device as 00h.

Latency Timer (0Dh, R/W)

Latency timer					0	0	0
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:3	LT	Number of clocks times 8.
2:0	–	Read-only. Returns 0s when read.

Header Type (0Eh, R)

SM	Configuration space layout						
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	SM	Single-/multi-function device. The Maestro-2E supports single-function operation. 0 = Single-function device.
6:0	CSL	Configuration space layout. Read-only. Defines layout for bytes 10h and up of the PCI configuration space header. Maestro-2E supports a 00h header type.

BIST Capability (0Fh, R)

Built-in self test capability							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	BIST	Built-in self test capability is 00h.

Maestro-2E I/O Space Base Address (10h, 11h, R/W)

IOSB[15:8]								0	0	0	0	0	0	0	ISI
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:8	IOSB[15:8]	I/O space base address. 256-Byte I/O space.
7:1	–	Reserved. Always write 0.
0	ISI	I/O space indicator. Hardwired to 1.

Subsystem Vendor ID (2Ch, 2Dh, R)

Subsystem vendor ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	SVID	Read/write protected. Customizable through register programming. Default = 125Dh. Writable when PCI 50h[0] = 1.

Subsystem ID (2Eh, 2Fh, R)

Subsystem ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	SID	Read/write protected. Customizable through register programming. Default = 1978h. Writable when PCI 50h[0] = 1 or through external strap pin 49. When pin 49 (GPIO4) is pulled down, the subsystem ID = 1978h.

Capability Pointer (34h, R)

Capability pointer							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	CP	This register provides a pointer into the PCI configuration header where the PCI power management register block resides. PCI header doublewords at pointer+0h and pointer+4h provide the power management (PM) registers. Each socket has its own capability pointer register. This register is read-only and returns C0h when read.

Interrupt Line (3Ch, R/W)

Interrupt line							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	IL	Interrupt line routing information. Indicates which system interrupt pin the Maestro-2E is connected to. The POST software writes the routing information to the Interrupt Line register as the system is initialized and configured. The value in this register depends on the system architecture. In x86-based PC systems, the values of 0 to 15 correspond with IRQ numbers 0 through 15, and the values from 16 to 254 are reserved. The value of 255 (Maestro-2E's default power-up value) signifies either "unknown" or "no connection" for the system interrupt. In the Maestro-2E, the default value is FFh. Bits [4:0] are read/write. Bits [7:5] = bit [4].

Interrupt Pin (3Dh, R)

Interrupt pin							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	IP	Interrupt pin information. Indicates which interrupt pin the Maestro-2E is using. This register is read-only and returns 01h when read, which indicates INTA#.

Minimum Grant (3Eh, R)

Minimum grant							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	MG	Min_Gnt. Identifies the burst period needed. This register is read-only and returns 02h when read, which corresponds to 500 ns.

Maximum Latency (3Fh, R)

Maximum latency							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	ML	Max_Lat. Identifies how often bus access is needed. This register is read-only and returns 18h when read, which corresponds to 6 ms.

Legacy Audio Control (40h, 41h, R/W)

LA	SIR	MIDIIRQ			SBIRQ			DMACH		IA	MQ	MI	GM	FM	SB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15	LA	Legacy audio disable. 1 = Disable legacy audio (default). 0 = Enable legacy audio.
14	SIR	Serial IRQs enable. 1 = Enable serial IRQs. 0 = Disable serial IRQs (default).
13:11	MIDIIRQ	MIDI I/O IRQ select. Read-only. Default to 010.
10:8	SBIRQ	Sound Blaster IRQ select. Bit 10 / Bit 9 / Bit 8 / IRQ Selection 0 / 0 / 0 / IRQ5 (default) 0 / 0 / 1 / IRQ7 0 / 1 / 0 / IRQ9 0 / 1 / 1 / IRQ10 1 / x / x / Reserved
7:6	DMACH	Sound Blaster DMA channel select. Bit 7 / Bit 6 / DMA Channel Selection 0 / 0 / Channel 0 0 / 1 / Channel 1 (default) 1 / 0 / Reserved 1 / 1 / Channel 3
5	IA	I/O address aliasing control. 1 = Enable address aliasing (default). Selects 10-bit I/O. 0 = Disable address aliasing.
4	MQ	MPU-401 IRQ enable. 1 = Enable MPU-401 IRQ (default). 0 = Disable MPU-401 IRQ.
3	MI	MPU-401 I/O enable. 1 = Enable MPU-401 I/O (default). 0 = Disable MPU-401 I/O.
2	GM	Game port enable. 1 = Enable game port (default). 0 = Disable game port.
1	FM	FM synthesis enable. 1 = Enable FM synthesis (default). 0 = Disable FM synthesis.
0	SB	Sound Blaster enable. 1 = Enable Sound Blaster channel (default). 0 = Disable Sound Blaster channel.

Legacy Audio Support

The Maestro-2E supports the following legacy audio addresses.

Table 3 Supported Legacy Audio Addresses

Legacy Audio Resources	I/O Address Base
Sound Blaster Pro	220h/240h
FM synthesis	388h
MPU-401	300h/320h/330h/340h
DMA	Channel 0, 1, 3
IRQ	5, 7, 9, 10

Maestro-2E Configuration A (50h, 51h, R/W)

SBI	PIC1	PIC0	GM	SG	DMAP	PW	IEM	R	M4D	S2	SD	S(V)ID
15	14	13	12	11	10 9 8	7	6	5	4 3	2	1	0

Bit Definitions:

Bits	Name	Description
15	SBI	Sound Blaster IRQ mask. 1 = Set this bit to enable IRQ masking when bit [10] = 1.
14	PIC1	PIC snoop mode 1. 1 = Set this bit in DOS mode when Maestro PCI IRQ is not assigned to IRQ5/7/9/10.
13	PIC0	PIC snoop mode 0. 1 = Set this bit in DOS mode when Maestro PCI IRQ is assigned to IRQ5/7/9/10.
12	GM	High-performance game port mode enable. 1 = Enable game port. 0 = Disable game port.
11	SG	Safe guard in TDMA mode, when bits [10:8] = 001. 1 = Set this bit to enable ISA merge during IOR 08h. ISA write-back in AutoDMA mode, when bits [10:8] = 100. 1 = Set this bit to enable ISA write-back in AutoDMA mode.
10:8	DMAP	ISA DMA policy. Bit 10 Bit 9 Bit 8 DMA Policy 0 0 0 Distributed DMA 0 0 1 Transparent DMA 0 1 0 PC/PCI DMA 0 1 1 Reserved 1 0 0 ISA write-back every 16 transfers 1 0 1 ISA write-back every 4 transfers 1 1 0 ISA write-back every 2 transfers 1 1 1 ISA write-back every transfer
7	PW	EN_PW. Posted write enable. 1 = Enable Maestro-2E posted write. 0 = Disable Maestro-2E posted write.
6	IEM	Emulate ISA timing on PCI. 1 = Use PCI timing. 0 = Emulate ISA timing.
5	–	Reserved. Always write 0.
4:3	M4D	MPU_401_DECODE. Bit 4 Bit 3 MPU-401 I/O 0 0 33x 0 1 30x 1 0 32x 1 1 34x
2	S2	SB240. Sound Blaster decode. 1 = Sound Blaster decode is 24x. 0 = Sound Blaster decode is 22x.
1	SD	Subtractive decoding. Write: 1 = Delay PCI grant by 1 clock during PCI master cycle and enable the detection of PCI subtractive decoding. Read: 1 = Subtractive decoding is detected.
0	SID	Write-enable bit for PCI subsystem ID (SID) and subsystem vendor ID (SVID). 1 = SID and SVID are read/write. 0 = SID and SVID are read-only (default).

Maestro-2E Configuration B (52h, 53h, R/W)

ICx	CIS	CxS	PMC	CLKSL	S EN	HWV	DHE	HVI	DE	R	R	R
15	14	13 12	11	10 9	8	7	6	5	4	3 2	1	0

Bit Definitions:

Bits	Name	Description
15	ICx	Internal clock multiplier enable. 1 = Enable internal clock multiplier. 0 = Disable internal clock multiplier.
14	CIS	Maestro-2E clock input select. 1 = Select the clock from the internal clock multiplier. 0 = Select the clock from an external crystal oscillator.
13:12	CxS	Clock multiplier mode select. Bit 13 Bit 12 Mode 0 0 Mode 0 0 1 Mode 1 1 0 Mode 2 1 1 Mode 3
11	PMC	Power management control for CLKRUN# enable. 1 = Enable PM control for CLKRUN#. 0 = Disable PM control for CLKRUN#.
10:9	CLKSL	Clock divider select for Sound Blaster. Bit 10 Bit 9 Clock Divider 0 0 Divided by 48 0 1 Divided by 49 1 0 Divided by 50 1 1 Reserved
8	S EN	S/PDIF enable. 1 = Enable S/PDIF output. 0 = Disable S/PDIF output (default).

Bits	Name	Description
7	HWV	Hardware volume control enable. 1 = Enable hardware volume control. 0 = Disable hardware volume control.
6	DHE	Reduced debounce for hardware volume control enable. 1 = Enable reduced debounce. 0 = Disable reduced debounce.
5	HVI	Up/down hardware volume button input select. 1 = Select input from GD[7:6]. 0 = Select input from GPIO[5:4].
4	DE	DSP interface enable. 1 = Enable the DSP interface/CHI bus. 0 = Disable the DSP interface/CHI bus.
3:2	–	Reserved.
1	–	Reserved. Always write 0.
0	–	Reserved.

ACPI Control A (54h, 55h, R/W)

12	24	978	SPDIF	GLUE	R	PIF	HV	GPIO	ASSP	SB	FM	RB	MIDI	GP	WP
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

The ACPI Control A register sets the state (D1 or D2) of the stop clock for each module (12 MHz clocks, 24 MHz clocks, ES978, SPDIF, GLUE, PCI interface, hardware volume, GPIO, ASSP interface, Sound Blaster, FM, ring bus/AC-link, MIDI, game port, and Wave Processor).

Bit Definitions:

Bits	Name	Description
15	12	ACPI stop clock control for the 12 MHz clock to the secondary CODEC output. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
14	24	ACPI stop clock control for the 24 MHz clock to the C24 output. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
13	978	ACPI stop clock control for the ES978. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
12	SPDIF	ACPI stop clock control for SPDIF. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
11	GLUE	ACPI stop clock control for GLUE. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
10	–	Reserved.
9	PIF	ACPI stop clock control for the PCI interface. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
8	HV	ACPI stop clock control for HW volume control. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
7	GPIO	ACPI stop clock control for GPIO. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
6	ASSP	ACPI stop clock control for the ASSP interface. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
5	SB	ACPI stop clock control for Sound Blaster. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
4	FM	ACPI stop clock control for FM. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
3	RB	ACPI stop clock control for Ring Bus/AC-link. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
2	MIDI	ACPI stop clock control for MIDI. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
1	GP	ACPI stop clock control for the game port. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
0	WP	ACPI stop clock control for the Wave Processor. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.

ACPI Control B (56h, 57h, R/W)

12	24	978	SPDIF	GLUE	R	PIF	HV	GPIO	ASSP	SB	FM	RB	MIDI	GP	WP
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

The ACPI Control B register enables the clock at the state (D1 or D2) set for each module in the ACPI Control A register.

Bit Definitions:

Bits	Name	Description
15	12	ACPI stop clock enable for the 12 MHz clock to the secondary CODEC output. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
14	24	ACPI stop clock enable for the 24 MHz clock to the C24 output. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
13	978	ACPI stop clock enable for the ES978. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
11	SPDIF	ACPI stop clock enable for SPDIF. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
11	GLUE	ACPI stop clock enable for GLUE. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
10	–	Reserved.

Bits	Name	Description
9	PIF	ACPI stop clock enable for the PCI interface. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
8	HV	ACPI stop clock enable for hardware volume control. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
7	GPIO	ACPI stop clock enable for GPIO. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
6	ASSP	ACPI stop clock enable for the ASSP interface. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
5	SB	ACPI stop clock enable for Sound Blaster. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
4	FM	ACPI stop clock enable for FM. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
3	RB	ACPI stop clock enable for Ring Bus/AC-link. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
2	MIDI	ACPI stop clock enable for MIDI. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
1	GP	ACPI stop clock enable for the game port. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
0	WP	ACPI stop clock enable for the Wave Processor. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.

User Configuration A (58h, 59h, R/W)

R	A:R B:GP	A:R B:NG	A:R B:MV	A:R B:×2	R	12	SC24	MIDI	3C24	3OB	978HV	978F	SO	×2
15 14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:14	–	Reserved.
13	A:R B:GP	REV A: Reserved. REV B: ES978 game port select. 1 = Select ES978 game port when docked. 0 = Select local game port.
12	A:R B:NG	REV A: Reserved. REV B: Non-glitch masking on 49.152 MHz clock input enable. 1 = Enable non-glitch masking.
11	A:R B:MV	REV A: Reserved. REV B: ES978 mixer volume control disable. 1 = Disable ES978 mixer volume control.
10	A:R B:×2	REV A: Reserved. REV B: 2nd PCI ×2 arbiter enable. 1 = Enable 2nd PCI ×2 arbiter.
9	–	Reserved.
8	12	Default = 0. 1 = Select 12 MHz input clock to clock multiplier from divider of external 49.152 MHz crystal input.
7	SC24	Default = 0. 1 = Disable stop clock for C24 output buffer at any power state.
6	MIDI	Default = 0. 1 = Enable delay of MIDI data transmit when docked.
5	3C24	Default = 0. 1 = Enable tri-state of C24 output buffer at D3 state.
4	3OB	Default = 0. 1 = Enable tri-state of output buffers (except C24) at D3 state.
3	978HV	Default = 0. 1 = Enable ES978 hardware volume control.
2	978F	Default = 0. 1 = Enable ES978 function.
1	SO	1 = Route SPDIF output to GPIO11 (pin 62). 0 = Route SPDIF output to GPIO3 (pin 48) (default).
0	×2	Default = 0. REV A: 1 = Enable 1st and 2nd PCI ×2 arbiter. REV B: 1 = Enable 1st PCI ×2 arbiter.

Distributed DMA Control (60h, 61h, R/W)

DMA[15:4]	0	0	0	DE
15 14 13 12 11 10 9 8 7 6 5 4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:4	DMA[15:4]	Distributed DMA base address.
3:1	–	Always write 0.
0	DE	Distributed DMA enable. 1 = Enable distributed DMA. 0 = Disable distributed DMA.

Capability ID (C0h, R)

Capability ID							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	CID	This register identifies the linked list item as the register for PCI power management. This register is read-only and returns 01h when read, which is the unique ID assigned by the PCI SIG for the PCI location of the capabilities pointer and the value.

Next-Item Pointer (C1h, R)

Next-Item pointer							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NIP	This register is used to indicate the next item in the linked list of the PCI power management capabilities. Since Maestro-2E functions only include one capabilities item, this register is read-only and returns 00h when read.

Power-Management Capabilities (C2h, C3h, R)

0	1	1	1	0	1	1	0	0	0	1	0	0	0	1	0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:11		PME_Support. This five-bit field indicates the power states in which the function may assert PME#. A value of 0 for any bit indicates that the function is not capable of asserting the PCE# signal while in that power state. Bit [15] = 0. PME# cannot be asserted from $D3_{cold}$. Bit [14] = 1. PME# can be asserted from $D3_{hot}$. Bit [13] = 1. PME# can be asserted from D2. Bit [12] = 1. PME# can be asserted from D1. Bit [11] = 0. PME# cannot be asserted from D0. Value of bits 15:11 = 01110.
10		D2_Support. This bit indicates that this function supports the D2 power management state. Value of bit 10 = 1.
9		D1_Support. This bit indicates that this function supports the D1 power management state. Value of bit 9 = 1.
8:6	–	Reserved. Value of bits 8:6 = 000.
5		DSI. The Device Specific Initialization bit indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. Value of bit 5 = 1.
4		Reserved. Value of bit 4 = 0.
3		PME clock. This bit indicates that no PCI clock is required for the function to generate PME#. Value of bit 3 = 0.
2:0		Version. This 3-bit field indicates that this function complies with Revision 1.0 of the PCI Power Management Interface specification. Value of bits 2:0 = 010.

Power-Management Control/Status (C4h, R)

0	0	0	0	0	0	PWR STATE	
7	6	5	4	3	2	1	0

The default value of this register 00h. This register determines and changes the current power state of the Maestro-2E function. The contents of this register are not affected by the internally-generated reset caused by the transition from the $D3_{hot}$ to D0 state.

Bit Definitions:

Bits	Name	Description
7:2	–	Bits [7:2] are read-only and return 0 when read.
1:0	PS	Power state. This 2-bit field is used both to determine the current power state of a function, and to set the function into a new power state. This field is encoded as: Bit 1 / Bit 0 / Power State 0 / 0 / D0 0 / 1 / D1 1 / 0 / D2 1 / 1 / $D3_{hot}$

PME Control (C5h, R/W)

PME ST	0	0	0	0	0	0	PME EN
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	PME ST	PME# status. Write: 1 = Clear PME# status. Read: 1 = PME# is active.
6:1	–	Bits [6:1] are read-only and return 0 when read.
0	PME EN	PME# enable. 1 = Enable PME. 0 = Disable PME.

WAVECACHE

The WaveCache dynamically prefetches from the system memory and manages samples for the Wave Processor (WP). The WaveCache is capable of handling up to 64 separate data streams for the WP. The types of different data streams supported include 16-bit mono, 16-bit stereo, 8-bit mono, 8-bit stereo, and 8-bit differential. The WaveCache also interfaces with the Task-Oriented Signal Processor (TOSP) to handle FM synthesis data streams.

Applicable Registers

Address	Name
Maestro2E_Base +10h, +11h	WaveCache Index register
Maestro2E_Base+12h, +13h	WaveCache Data register
Maestro2E_Base+14h,+15h	WaveCache Control register

WaveCache Configurations

The WaveCache has three different configurations:

- WP configuration
- TOSP configuration
- Test configuration

These configurations are set by WaveCache Control register bits [0], and [9:7].

The primary configuration, the WP configuration, is where the WaveCache manages samples for the WP. The CPU may write into WaveCache Control registers or WaveCache channel buffers using the WaveCache Index and Data register.

In the TOSP configuration, the WaveCache serves as a general-purpose data buffer for the TOSP. Only the TOSP may access the WaveCache in this configuration.

The Test configuration is for device test purposes, in which only the CPU may read/write the WaveCache. It is enabled by setting bit [0] of the WaveCache control register to 1.

WaveCache Access

The host may access the WaveCache with limitations using the WaveCache Index and Data registers. By setting up the Index register first, the actual read/write to and from the WaveCache registers occur when the indexed data register is read or written. The host may write to the WaveCache in either WP configuration or Test configuration modes, but may only read from the WaveCache when in Test configuration mode.

Table 4 WaveCache Indexed Data Registers

Index	Register
1F4 – 1FF	Wavetable Base Address register 1:0
1F0 – 1F3	PCM/Status FIFO Base Address register 3:0
n* (08 hex)	Channel n Control register, n = 61:0
other locations	Channel buffers

Wavetable Base Address (R/W)

Data[27:12]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

There are a total of twelve Wavetable Base Address registers. Up to four disjoint table addresses can be specified in these twelve registers. The purpose of these registers is to allow the WP channels to deal with only logical addresses.

The Maestro-2E supports wavetable sizes from 1 MB to 8 MB in system memory. This wavetable is divided into four equal sizes and these wavetable quarters can reside in physically disjoint locations mapped by the twelve base address registers. Depending on the different wavetable sizes, different top channel address bits (2 bits) are used to select the corresponding base address register and thus the quarter wavetable. Physical address is calculated by adding the base address and the WP address together.

Table 5 WaveCache Top Channel and Physical Address

Top Channel Address Bits	Physical Address
WPWA[1][18:15] (1 MB)	m = 14 (1 MB)
WPWA[19:16] (2 MB)	m = 15 (2 MB)
WPWA[20:17] (4 MB)	m = 16 (4 MB)
WPWA[21:18] (8 MB)	m = 17 (8 MB)
0000	WTBAR0[27:12] + WPWA[m:0][2]
0001	WTBAR1[27:12] + WPWA[m:0]
0010	WTBAR2[27:12] + WPWA[m:0]
0011	WTBAR3[27:12] + WPWA[m:0]
0100	WTBAR4[27:12] + WPWA[m:0]
0101	WTBAR5[27:12] + WPWA[m:0]
0110	WTBAR6[27:12] + WPWA[m:0]
0111	WTBAR7[27:12] + WPWA[m:0]
100-	WTBAR8[27:12] + WPWA[m+1:0]
101-	WTBAR9[27:12] + WPWA[m+1:0]
110-	WTBAR10[27:12] + WPWA[m+1:0]
111-	WTBAR11[27:12] + WPWA[m+1:0]

1. WPWA (WP WaveSpace Address) is measured in words.
2. When the WaveCache adds WTBARn addresses (bytes) and WPWA addresses (words), its address mapping hardware automatically performs the necessary shifting.

PCM/Status FIFO Base Address (R/W)

PCM/Status FIFO base address[27:12]															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 6 PCM Top Channel and Physical Address

Top Channel Address Bits	Physical Address
WPWA[1][22:21]	m = 20
00	PCMBAR0[27:12] + WPWA[m:0][2]
01	PCMBAR1[27:12] + WPWA[m:0]
10	PCMBAR2[27:12] + WPWA[m:0]
11	PCMBAR3[27:12] + WPWA[m:0]

1. WPWA (WP WaveSpace Address) is measured in words.
2. When the WaveCache adds PCMBARn addresses (bytes) and WPWA addresses (words), its address mapping hardware automatically performs the necessary shifting.

The PCM/Status FIFO Base Address register is used in one of the following two situations:

3. The WP writes status information to the System Status FIFO.
4. WPWA22 is ‘1’ in accessing system memory.

Channel Control for Channels 0-61 (R/W)

Tag address[15:3]													8B	SA	DA
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:3	TA	Address tag. Before a WP channel is activated, an invalid tag address must be loaded into the Tag address bits. Tag address[15:3] corresponds to physical address [15:3]. An invalid tag is an address that is at least 10 hex away from the starting sample address of the channel. For example, if a channel is accessing samples in: – incremental address style: [Channel starting address - 10h] can be written to bits [15:3]. – decremental address style: [Channel starting address +10h] can be written to bits [15:3].
2	8B	8-Bit format. To play 8-bit unsigned-magnitude samples, set bit [2]. In this format, MSB bits [15] and [7] of the input samples are toggled.
1	SA	Stereo format. 1 = Channel samples are in interleaved stereo format. Left and right samples are confined to paired adjacent channels. For example: channels 0/1 are stereo paired channels, and channels 1/2 are not. The SA bits of both paired channels must be set to 1.
0	DA	Decremental addressing. 1 = Channel is accessing samples in decremental address order. 0 = Channel is accessing samples in incremental address order.

Programming the WaveCache

The outlined steps for programming the WaveCache are:

1. Determine the size and locations of the wavetable in system memory.
2. Program the WaveCache Control register:
   – WaveCache configuration = WP configuration
   – Wavetable size
   – EN_WaveCache = 1
3. Program the Wavetable Base Address registers.
4. Program the WP channels:
   – Program Channel Control register for the following:
   data format
   incremental/decremental addressing
   invalid tag address
   – Program the WP Channel Parameter registers
5. Repeat step 4 for all channels.

CODEC / MIXER INTERFACE

The Maestro-2E supports the AC'97 CODEC mode, which supports interface to AC97-compliant CODECs.

Applicable Registers

Address	Name
Maestro2E_Base +30h	CODEC Command/Status
Maestro2E_Base +32h, +33h	CODEC Data register

AC'97 Interface

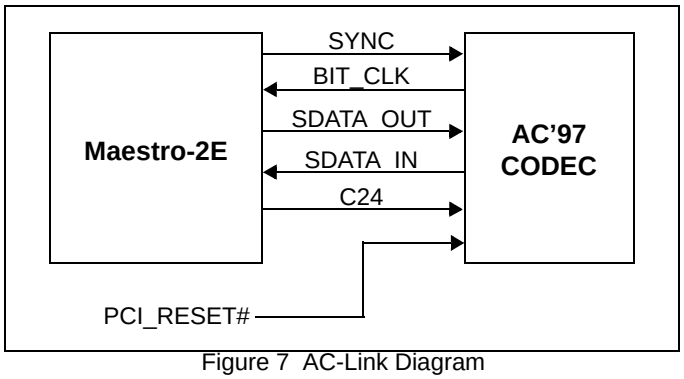


Figure 7 AC-Link Diagram

AC'97 Serial Interface Timing

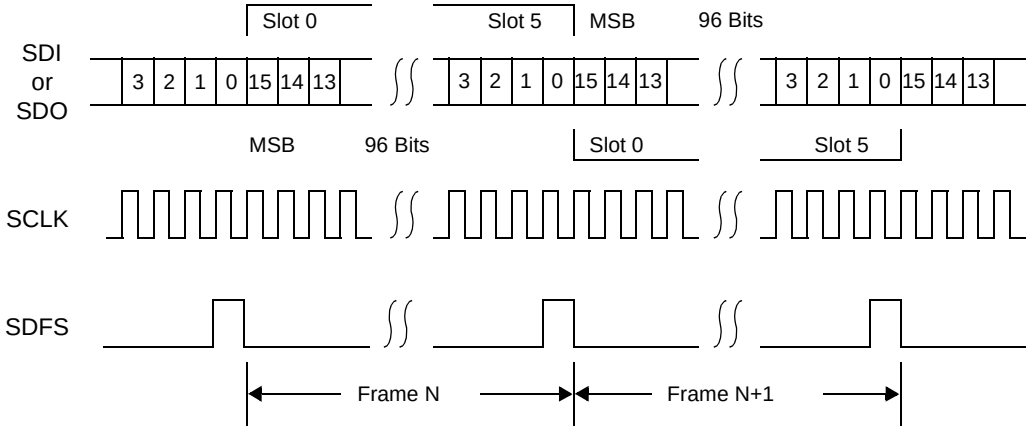


Figure 8 Serial Interface Timing

APPLICATION SPECIFIC SIGNAL PROCESSOR

Applicable Registers

Address	Name
Maestro2E_Base +80h, +81h	ASSP Memory Index Port
Maestro2E_Base +82h, +83h	ASSP Memory Port
Maestro2E_Base +84h, +85h	ASSP Data Port
Maestro2E_Base +A2h	ASSP Control A register
Maestro2E_Base +A4h	ASSP Control B register
Maestro2E_Base +A6h	ASSP Control C register
Maestro2E_Base +A8h	Host Write Index register
Maestro2E_Base +AAh	Host Write Data register
Maestro2E_Base +ACh	ASSP to Host IRQ Status register

ASSP Memory Mapping

ASSP can access internal memory only. There are 2 Kwords of space for program usage and 3 Kwords of space for data usage (excluding the WaveCache).

Table 7 ASSP Memory Mapping

Type of Memory	Addresses	Description
Program memory	0h – 3FFh	1 KW SRAM
	0800h – 0BFFh	1 KW SRAM
Data memory	400h – 5FFh	512 W WaveCache
	1000h – 17FFh	2 KW SRAM
	2000h – 23FFh	1 KW SRAM

ASSP I/O Mapping

Table 8 ASSP I/O Mapping

Addresses	Description
0000h – 0FFFh	FM
1000h – 1FFFh	Hardware volume status input
2000h – 2FFFh	Ring bus input full even DWord = left, odd DWord = right
3000h – 3FFFh	Ring bus output empty even DWord = left, odd DWord = right
4000h – 4FFFh	ASSP DMA I/O port
5000h – 5FFFh	ASSP-to-host IRQ
6000h – 6FFFh	I^2S time stamp input
7000h – 7FFFh	I^2S data input even DWord = left, odd DWord = right
8x00h – 8x03h	DSP/CHI bus data input/output
8x08h – 8x0Bh	ADCL (read); PCM Center (write)
8x0Ch – 8x0Fh	ADCR (read); PCM Left surround (write)
8x10h – 8x13h	MIC (read); PCM Right surround (write)
8x14h – 8x17h	Modem status (read); PCM LFE (write) Modem status: bit 0: Line1 out; bit 1: Line2 out; bit 2: Handset out; bit 4: Line1 in; bit 5: Line2 in; bit 6: Handset in
8x20h – 8x23h	Line1 in (read); Line1 out (write)
8x24h – 8x27h	Line2 in (read); Line2 out (write)
8x28h – 8x2Bh	Handset in (read); Handset out (write)
A000h – AFFFh	ASSP stop clock
B000h – BFFFh	SPDIF data read/write

ASSP DMA Control Registers

Host DMA Base Address Low (IO 4000h, W)

A[15:2]	Reserved

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:2	A[15:2]	Dword address corresponding to A[15:2] of the system memory.
1:0	–	Reserved. Fixed at 0 for Dword addressing.

Host DMA Base Address High (IO 4001h, W)

Reserved	A[27:16]

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:12	–	Reserved. Fixed at 0h for Dword addressing.
11:0	A[27:16]	Dword address corresponding to A[27:16] of the system memory.

ASSP DMA Base Address (IO 4002h, W)

R	R/W	Reserved	Offset

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

An IO write cycle to 4002h triggers the ASSP DMA transfer.

The ASSP DMA base address is fixed at 1300h in data memory by default. A 6-bit offset extends the address range from 1000h to 13F0h.

Each ASSP DMA transfer is fixed at 32 bytes.

Bit Definitions:

Bits	Name	Description
15	–	Reserved.
14	R/W	Read/write host/ASSP memory. 1 = Read ASSP memory; write host memory. 0 = Read host memory; write ASSP memory.
13:6	–	Reserved.
5:0	Offset	Offset address from the ASSP DMA base address

Data Transfer Between ASSP and Host Memories

The Maestro-2E supports two methods of data transfer between ASSP and host memory. CPU access through 32-bit IO is supported for small transfers. For large transfers, DMA is supported for transferring data to and from ASSP memory. Both the ASSP program and data memory spaces are accessible using these two methods. DMA operation can also be used for dynamic downloading of ASSP programs. Both types of transfer put the ASSP in a hold state.

32-Bit I/O Transfer Operation

To perform an IO transfer between the CPU and the ASSP:

1. Program the ASSP Memory Index port (Maestro2E_Base +80h, +81h) with the ASSP starting address in word boundary using 16-bit IO.
2. Set the ASSP Memory port (Maestro2E_Base +82h, +83h) bits [1:0] to select either program or data memory. See Table 9 for the settings.
3. Send a 32-bit read or write IO operation to the ASSP Data port (Maestro2E_Base +84h, +85h) starting with the programmed ASSP address programmed in step 1. 16-Bit IO operations are not supported. The ASSP Memory Index port auto-increments for subsequent IO operations.

DMA Transfer Operation

The following explains how to set up the ASSP to perform DMA between the Host and the ASSP. The ASSP controls the DMA operation by writing to I/O ports 4000h to 4002h.

1. The low 16 bits and the high 16 bits of the host memory base address are written into I/O ports 4000h and 4001h.
2. I/O port 4002h bit [14] controls the direction of the DMA operation by specifying whether it is from the host memory or from the ASSP memory. Bits [2:0] control the offset address from the DSP DMA base address.
3. At the end of the DMA transfer, the END of ASSP DMA interrupt is sent to the ASSP.

Each DSP DMA transfer is fixed at 32 bytes.

Table 9 ASSP Address Map

ASSP Transfer Address [17:16]	Mapped ASSP Resources
10	Program memory
11	Data memory

Messaging Between the CPU and the ASSP

Outside of DMA transfers, the CPU can send messages to the ASSP with associated interrupts to the ASSP. The messages are sent through two 8-bit registers:

- Host Write Index register
- Host Write Data register

The ASSP receives an interrupt whenever the Host Write Data register is written by the CPU. The ASSP can read the data and the index sent by the CPU from the I/O port.

The ASSP can generate one of eight software interrupts to the CPU. The CPU may examine the ASSP Interrupt Status register to determine the nature of the interrupt.

ASSP Interrupts

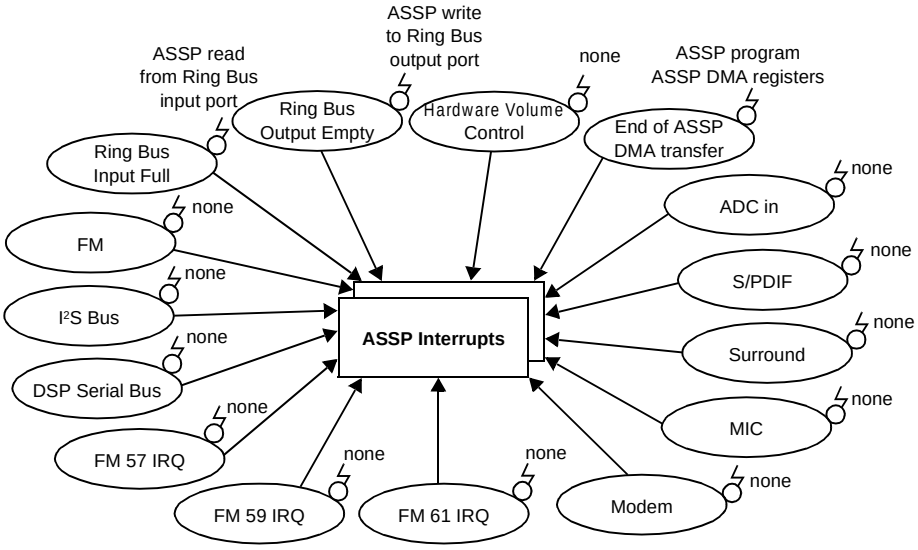


Figure 9 ASSP Interrupt Map

Table 10 ASSP Interrupts

Interrupt	Function	Interrupt	Function
0	ASSP reset	8	ASSP FM channel 57 IRQ
1	ASSP FM	9	ASSP FM channel 59 IRQ
2	ASSP hardware volume control	10	ASSP FM channel 61 IRQ
3	ASSP ADC input	11	ASSP DSP serial bus input/output
4	ASSP S/PDIF	12	ASSP I²S input
5	ASSP ring bus input full	13	ASSP surround
6	ASSP ring bus output empty	14	ASSP MIC
7	ASSP end of ASSP DMA transfer	15	ASSP Modem

ES978 DOCKING INTERFACE

When docked, the Maestro-2E and the AC'97 CODEC are in constant communication with the ES978 in the expansion unit. A half-duplex, bidirectional digital control link keeps the Maestro-2E updated on the ES978's status and vice versa.

Table 11 ES978 Interface Pins

Pin	Description
XSC	Expansion serial bus clock. XSC is selected by setting PCI 58h[2] = 1 while the DOCKED pin = 1.
XSD	Expansion serial bus data I/O. XSD is selected by setting PCI 58h[2] = 1 while the DOCKED pin = 1.
DOCKED	Status input that is active-high when the Maestro-2E interfaces with an AC'97 CODEC docked to the ES978.

Two wires are used to transmit serial data between the Maestro-2E and ES978. The first signal, XSC, acts as a frame sync and shift clock. The bit clock rate is 3.07 MHz.

A typical frame consists of:

- Sync period – 24 clocks wide
- Download period – 144 clocks wide
- Turnaround period – 8 clocks wide
- Upload period – 80 clocks wide

Total: 256 bit clocks/frame, which is equivalent to a 12 kHz frame rate.

The function of the upload and download periods is to continually update corresponding registers within each device. For example, pressing the VOLUP button in the expansion unit, transmits the pin state to the Maestro-2E where it is AND'ed with the same pin of the Maestro-2E. Bit[3] of PCI Configuration register 58h must be set to 1 to enable the ES978 hardware volume control. The Maestro-2E updates its copy of the master volume register. The ES978 receives the new value in the master volume register during the first download period of the next frame.

Sync Period

In the sync period, XSC is low for 12 bit clock periods, and then high for 12 bit clock periods.

Download Period

In the download period, data is transmitted serially from the Maestro-2E to the ES978 through the signal XSD. XSC is the bit shift clock. Data is shifted out of the Maestro-2E on the falling edge of XSC. Data is shifted into the ES978 on the rising edge of XSC.

The download period is 144 bits wide. The last 8 bits are a checksum byte.

The upload period is 80 bits wide. The last 8 bits are a checksum byte.

Table 12 contains the data configuration for the download period (from the Maestro-2E to the ES978).

Turnaround Period

There are 8 bits between the end of the download period and the start of the upload period.

Upload Period

In the upload period, data is transmitted serially in the opposite direction, from the ES978 to the Maestro-2E through the same signal wire, XSD.

Table 13 contains the data configuration for the upload period (from the ES978 to the Maestro-2E).

Other Register Bits

The read-only position register is located at Maestro2E_Base+D2h and Maestro2E_Base+D4h. Bits [4:0] of Maestro2E_Base+D2h is the byte number for the current position. When set to 1, bit [0] of Maestro2E_Base+D2h is the software reset for interface logic. When set to 0, operation is normal (default).

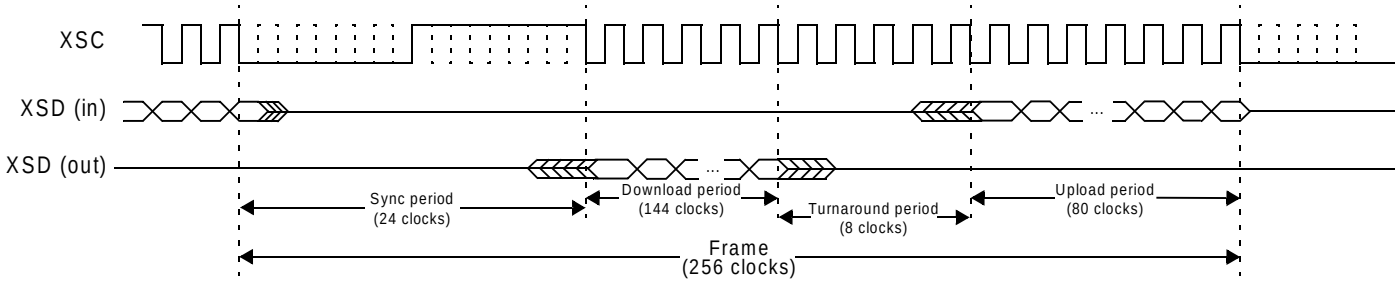


Figure 10 Expansion Audio Interface Timing

Table 12 Download Period Data Configuration (From the Maestro-2E to the ES978)

Bits	Function	Offset	Read/Write
1:0	Mode of expansion analog interface	Maestro2E_Base+C0h	Read/write by host
4:2	Record source select		Read/write by host
5	Master output enable		Read/write by host
6	MIDI loopback test		Read/write by host
7	MIDI transmit signal		Read-only by host; Write by logic
15:8	MIDI transmit data	Maestro2E_Base+C1h	Read-only by host; Write by logic
23:16	XGPO[7:0] data	Maestro2E_Base+C2h	Read/write by host
31:24	Playback mixer – Host audio volume	Maestro2E_Base+C3h	Read/write by host
39:32	Playback mixer – Line volume	Maestro2E_Base+C4h	Read/write by host
47:40	Playback mixer – Mic volume	Maestro2E_Base+C5h	Read/write by host
55:48	Playback mixer – Aux A (CD) volume	Maestro2E_Base+C6h	Read/write by host
63:56	Playback mixer – Aux B volume	Maestro2E_Base+C7h	Read/write by host
71:64	Playback mixer – I^2S / ES689/ES69x volume	Maestro2E_Base+C8h	Read/write by host
79:72	Record mixer – Host audio volume	Maestro2E_Base+C9h	Read/write by host
87:80	Record mixer – Line volume	Maestro2E_Base+CAh	Read/write by host
95:88	Record mixer – Mic volume	Maestro2E_Base+CBh	Read/write by host
103:96	Record mixer – Aux A (CD) volume	Maestro2E_Base+CCh	Read/write by host
111:104	Record mixer – Aux B volume	Maestro2E_Base+CDh	Read/write by host
119:112	Record mixer – I^2S / ES689/ES69x volume	Maestro2E_Base+CEh	Read/write by host
127:120	Master volume left	Maestro2E_Base+CFh	Read/write by host
135:128	Master volume right	Maestro2E_Base+D0h	Read/write by host
143:136	CRC checksum	Maestro2E_Base+D1h	Read-only by host; Write by logic

Table 13 Upload Period Data Configuration (From the ES978 to the Maestro-2E)

Bits	Function	Offset	Read/Write
3:0	Joystick switch status	Maestro2E_Base+D5h	Read-only by host
4	VOLUP input status (active-low)		Read-only by host
5	VOLDN input status		Read-only by host
6	MUTE input status		Read-only by host
7	MIDI receive data following		Read-only by host
15:8	MIDI receive data	Maestro2E_Base+D6h	Read-only by host
23:16	XGPI input state	Maestro2E_Base+D7h	Read-only by host
31:24	Low byte joystick timer A	Maestro2E_Base+D8h	Read-only by host
39:32	Low byte joystick timer B	Maestro2E_Base+D9h	Read-only by host
47:40	Low byte joystick timer C	Maestro2E_Base+DAh	Read-only by host
55:48	Low byte joystick timer D	Maestro2E_Base+DBh	Read-only by host
59:56 63:60	High nibble joystick timer A High nibble joystick timer B	Maestro2E_Base+DCh	Read-only by host
67:64 71:68	High nibble joystick timer C High nibble joystick timer D	Maestro2E_Base+DDh	Read-only by host
79:72	CRC checksum	Maestro2E_Base+DEh	Read-only by host

I/O PORTS

Port Summary

Table 14 Maestro-2E I/O Port Summary

Function	Port		Register (Number of Bytes)	Notes
Direct Sound Processor	Maestro2E_Base	+00h	Data (2)	
		+02h	Index (2)	
		+04h	Interrupt Status (2)	
		+06h	Sample_Count (2)	Read-only
WaveCache	Maestro2E_Base	+10h	WaveCache Index (2)	
		+12h	WaveCache Data (2)	
		+14h	WaveCache Control (2)	
Host Interrupt	Maestro2E_Base	+18h	Host Interrupt Control (2)	
		+1Ah	Host Interrupt Status (1)	
Hardware Volume Control	Maestro2E_Base	+1Bh	Hardware Volume Control (1)	
		+1Ch	Shadow of Mixer for Voice (1)	
		+1Dh	HWV Counter for Voice (1)	
		+1Eh	Shadow of Mixer for Master (1)	
		+1Fh	HWV Counter for Master (1)	
High-Performance Game Port	Maestro2E_Base	+20h	Delay 0 (2)	
		+24h	Delay 1 (2)	
		+28h	Delay 2 (2)	
		+2Ch	Delay 3 (2)	
CODEC Interface	Maestro2E_Base	+30h	Command / Status (1)	
		+32h	Data (2)	
Ring Bus	Maestro2E_Base	+34h	Ring Bus Control (4)	
Modem Interface	Maestro2E_Base	+50h	DAA Data Input/Output (2)	
GPI/O General-Purpose I/O	Maestro2E_Base	+60h	GPIO Data (2)	
		+64h	GPIO Mask (2)	
		+68h	GPIO Direction (2)	
ASSP Application Specific Signal Processor	Maestro2E_Base	+80h	ASSP Memory Index Port (4)	
		+84h	ASSP Memory Data Port (2)	
		+A2h	ASSP Control register A (1)	
		+A4h	ASSP Control register B (1)	
		+A6h	ASSP Control register C (1)	
		+A8h	Host Write Index register (1)	
		+AAh	Host Write Data register (1)	
		+ACh	ASSP to Host Interrupt Status (1)	
Miscellaneous I/O Port	Maestro2E_Base	+90h	Game Port Addresses (8)	
		+98h	MPU-401 Port Addresses (4)	
		+9Ch	Clock Multiplier Data Ports (2)	
ES978 Docking Control	Maestro2E_Base	+C0h	ES978 Miscellaneous Control (1)	
		+C1h	MIDI Transmit Data (1)	
		+C2h	XGPO Data (1)	
		+C3h	Playback Mixer Addresses (6)	
		+C9h	Record Mixer Addresses (6)	
		+CFh	Master Volume Addresses (2)	
		+D1h	CRC Checksum Address (1)	

Port Descriptions

Data (Maestro2E_Base+00h, +01h, R/W)

Data															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	Data	Data.

Index (Maestro2E_Base+02h, +03h, R/W)

Index															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	Index	Index.

Interrupt Status (Maestro2E_Base+04h, +05h, R/W)

IRQ status															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	IRQ status	Interrupt status.

Sample_Count (Maestro2E_Base+06h, +07h, R)

Sample count															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	Sample count	Sample_count. Read-only.

WaveCache Index (Maestro2E_Base+10h, +11h, R/W)

0	0	0	0	0	0	0	WCA								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register requires 16-bit access.

Bit Definitions:

Bits	Name	Description
15:9	–	Reserved. Always write 0.
8:0	WCA	WaveCache index.

WaveCache Data (Maestro2E_Base+12h, +13h, R/W)

WCDA															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register requires 16-bit access.

Bit Definitions:

Bits	Name	Description
15:0	WCD	WaveCache data.

WaveCache Control (Maestro2E_Base+14h, +15h, R/W)

0	0	0	0	0	0	XCH	EW	CEN	WTS[1:0]	R	SGC	R	WT
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register requires 16-bit access.

Bit Definitions:

Bits	Name	Description
15:10	–	Reserved.
9	XCH	Channels 56/57, channels 58/59 enable. 1 = Enable ch56/57, ch58/59 as the extra playback/record channel. 0 = Disable ch56/57, ch58/59 as the extra playback/record channel.
8	EW	EN_WaveCache. WaveCache operation enable. 1 = Enable WaveCache operation. 0 = Disable WaveCache operation.
7	CEN	Channels 60/61 enable. 1 = Enable ch60/61 as the playback/record channels. 0 = Disable ch60/61 as the playback/record channels.
6:5	WTS	Wavetable size. Bit 6 / Bit 5 / Wavetable Size 0 / 0 / 1 MB 0 / 1 / 2 MB 1 / 0 / 4 MB 1 / 1 / 8 MB
4	–	Reserved.
3:2	SGC	Scatter and gather DMA control. Bit 3 / Bit 2 / Channels 0 / 0 / Disable 0 / 1 / Channels 40-47 are in SG mode; Channels 52-55 cannot read PCI memory through WaveCache 1 / 0 / Channels 32-47 are in SG mode; Channels 48-55 cannot read PCI memory through WaveCache 1 / 1 / Reserved
1	–	Reserved.
0	WT	WaveCache test mode enable. 1 = Enable WaveCache test mode. CPU may read/write WaveCache in this mode.

Host Interrupt Control
(Maestro2E_Base+18h, +19h, R/W)

MR	DR	R	PGE	R	CE	R	HIE	R	DIE	R	DSIE	MIE	SIE
15	14	13 12 11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15	MR	Maestro-2E software reset enable. 1 = Enable Maestro-2E software reset. 0 = Disable Maestro-2E software reset.
14	DR	DirectSound software reset enable. 1 = Enable DirectSound software reset. 0 = Disable DirectSound software reset.
13:11	–	Reserved.
10	PGE	Hardware volume control to PME# generation enable.
9	–	Reserved.
8	CE	CLKRUN# generation test mode enable. 1 = Enable CLKRUN# generation all the time. 0 = Disable CLKRUN# generation.
7	–	Reserved.
6	HIE	Hardware volume control interrupt enable. 1 = Enable hardware volume control interrupt. 0 = Disable hardware volume control interrupt.
5	–	Reserved.
4	DIE	ASSP software interrupt enable. 1 = Enable ASSP software interrupt. 0 = Disable ASSP software interrupt.
3	–	Reserved.
2	DSIE	DirectSound interrupt enable. 1 = Enable DirectSound interrupt. 0 = Disable DirectSound interrupt.
1	MIE	MPU-401 interrupt enable. 1 = Enable MPU-401 interrupt. 0 = Disable MPU-401 interrupt.
0	SIE	Sound Blaster interrupt enable. 1 = Enable Sound Blaster interrupt. 0 = Disable Sound Blaster interrupt.

Host Interrupt Status (Maestro2E_Base+1Ah, R/W)

R	IHWV	R	ID	R	4V	4M	BS
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	–	Reserved.
6	IHWV	Hardware volume control interrupt. 1 = Hardware volume control interrupt pending. 0 = No hardware volume control interrupt.
5	–	Reserved.
4	ID	ASSP software interrupt. 1 = ASSP interrupt pending. 0 = No ASSP interrupt.
3	–	Reserved.
2	4V	DirectSound interrupt. 1 = DirectSound interrupt pending. 0 = No DirectSound interrupt.
1	4M	MPU-401 receive interrupt. 1 = MPU-401 receive interrupt pending. 0 = No MPU-401 receive interrupt.
0	BS	Sound Blaster interrupt. 1 = Sound Blaster interrupt pending. 0 = No Sound Blaster interrupt.

Hardware Volume Control
(Maestro2E_Base+1Bh, R/W)

Reserved	Split
7 6 5 4 3 2 1	0

Bit Definitions:

Bits	Name	Description
7:1	–	Reserved.
0	Split	Hardware volume/counter control register split. 1 = Split volume register from counter register. 0 = Do not split volume from counter register.

Shadow of Mixer Register for Voice
(Maestro2E_Base+1Ch, R/W)

Voice volume left	HWML	Voice volume right	HWMR
7 6 5 4	3	2 1	0

Bit Definitions:

Bits	Name	Description
7:4	VVL	Voice volume left.
3	HWML	Hardware mute button pressed. 1 = Mute.
2:1	VVR	Voice volume right.
0	HWMR	Hardware mute button pressed. 1 = Mute.

HW Volume Control Counter for Voice (Maestro2E_Base+1Dh, R/W)

Voice volume left			HWML	Voice volume right			HWMR
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:4	VVL	Voice volume left.
3	HWML	Hardware mute button pressed. 1 = Mute.
2:1	VVR	Voice volume right.
0	HWMR	Hardware mute button pressed. 1 = Mute.

Shadow of Mixer Register for Master (Maestro2E_Base+1Eh, R/W)

Master volume left			HWML	Master volume right			HWMR
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:4	MVL	Master volume left.
3	HWML	Hardware mute button pressed. 1 = Mute.
2:1	MVR	Master volume right.
0	HWMR	Hardware mute button pressed. 1 = Mute.

HW Volume Control Counter for Master (Maestro2E_Base+1Fh, R/W)

Master volume left			HWML	Master volume right			HWMR
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:4	MVL	Master volume left.
3	HWML	Hardware mute button pressed. 1 = Mute.
2:1	MVR	Master volume right.
0	HWMR	Hardware mute button pressed. 1 = Mute.

Joystick 1 X-Delay (Maestro2E_Base+20h,+21h, R/W)

2A	2B	1A	1B	Delay[11:0]											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:12	2A/2B 1A/1B	Fire buttons.
11:0	Delay[11:0]	Timer delay in units of 2 microseconds.

Joystick 1 Y-Delay (Maestro2E_Base+24h,+25h, R/W)

2A	2B	1A	1B	Delay[11:0]											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:12	2A/2B 1A/1B	Fire buttons.
11:0	Delay[11:0]	Timer delay in units of 2 microseconds.

Joystick 2 X-Delay (Maestro2E_Base+28h,+29h, R/W)

2A	2B	1A	1B	Delay[11:0]											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:12	2A/2B 1A/1B	Fire buttons.
11:0	Delay[11:0]	Timer delay in units of 2 microseconds.

Joystick 2 Y-Delay (Maestro2E_Base+2Ch,+2Dh, R/W)

2A	2B	1A	1B	Delay[11:0]											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:12	2A/2B 1A/1B	Fire buttons.
11:0	Delay[11:0]	Timer delay in units of 2 microseconds.

CODEC Command / Status (Maestro2E_Base+30h, W)

RW	AD[6:0]						
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	RW	Read/Write. 1 = Read cycle. 0 = Write cycle.
6:0	AD[6:0]	CODEC register address.

CODEC Command / Status (Maestro2E_Base+30h, R)

0	0	0	0	0	0	0	ST
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:1	–	Reserved. Always read 0.
0	ST	Read/write status. 1 = CODEC register read/write is in progress. 0 = CODEC register read/write is done.

CODEC Data (Maestro2E_Base+32h,+33h, W)

WT CODEC Data[15:0]

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:0	WT	16 bits of data to be written to the CODEC.

CODEC Data (Maestro2E_Base+32h,+33h, R)

RD CODEC Data[15:0]

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:0	RD	16 bits of data read from the CODEC.

Ring Bus Destination Control Format (Maestro2E_Base+34h,+35h, R/W)

ADCL_DC	Reserved	DirectSound_DC	ASSP_DC

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:12	ADCL_DC	ADCL_DC[3] = (Bit [15]) Mono/stereo select. 1 = Stereo. 0 = Mono. ADCL_DC[2:0] Destination ID select. Bit 14 Bit 13 Bit 12 Destination ID 0 0 0 No destination 0 0 1 DAC 0 1 0 Reserved 0 1 1 Reserved 1 0 0 DirectSound input 1 0 1 ASSP input 1 1 0 Reserved 1 1 1 Reserved
11:8	–	Reserved.
7:4	DS_DC	DirectSound_DC[3] = (Bit [7]) Mono/stereo select. 1 = Stereo. 0 = Mono. DirectSound_DC[2:0] Destination ID select. Bit 6 Bit 5 Bit 4 Destination ID 0 0 0 No destination 0 0 1 DAC 0 1 0 Reserved 0 1 1 Reserved 1 0 0 DirectSound input 1 0 1 ASSP input 1 1 0 Reserved 1 1 1 Reserved
3:0	ASSP_DC	ASSP_DC[3] = (Bit [3]) Mono/stereo select. 1 = Stereo. 0 = Mono. ASSP_DC[2:0] Destination ID select. Bit 2 Bit 1 Bit 0 Destination ID 0 0 0 No destination 0 0 1 DAC 0 1 0 Reserved 0 1 1 Reserved 1 0 0 DirectSound input 1 0 1 ASSP input 1 1 0 Reserved 1 1 1 Reserved

Ring Bus Control A (Maestro2E_Base+36h,+37h, R/W)

I²S	DSP	ER	ES	LAC SDFS	LAC PME	RAC SDFS	RAC PME	Reserved

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15	I²S	I²S input enable. 1 = Enable I²S input. 0 = Disable I²S input.
14	DSP	DSP serial bus enable. 1 = Enable DSP serial bus. 0 = Disable DSP serial bus.
13	ER	EN_RING. Ring bus enable. 1 = Enable ring bus. 0 = Disable ring bus.
12	ES	Serial AC-link enable. 1 = Enable serial AC-link. 0 = Disable serial AC-link.
11	LAC SDFS	Driving SDFS of local AC-link enable. 1 = Enable driving SDFS of local AC-link. 0 = Disable driving SDFS of local AC-link.
10	LAC PME	Driving PME from SDI of local AC-link. 1 = Enable driving PME from SDI of local AC-link. 0 = Disable driving PME from SDI of local AC-link.
9	RAC SDFS	Driving SDFS of remote AC-link enable. 1 = Enable driving SDFS of remote AC-link. 0 = Disable driving SDFS of remote AC-link.
8	RAC PME	Driving PME from SDI of remote AC-link. 1 = Enable driving PME from SDI of remote AC-link. 0 = Disable driving PME from SDI of remote AC-link.
7:0	–	Reserved.

Ring Bus Control B (Maestro2E_Base+38h, R/W)

R	SSPE	CDC2	SPDIF	ITB	R	CDC ID	
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	–	Reserved.
6	SSPE	1 = Enable single set of pins for multiple CODECs. 0 = Enable single set of pins for dual CODECs.
5	CDC2	1 = Enable second AC98. 0 = Enable single AC9x.
4	SPDIF	1 = Enable SPDIF function.
3	ITB	1 = Disable invalidation of the tag bits for slots 1 and 2 for the second AC98.
2	–	Reserved.
1:0	CDC ID	Second CODEC ID. Bit 1 Bit 0 CODEC ID 0 0 Reserved 0 1 Reserved 1 0 AC98 1 1 Reserved

SDO Output Destination Control (Maestro2E_Base+3Ah, R/W)

I/O		HS		L2DAC		PCM R/LF		PCM CLS		L1DAC		PCM L/R		CA	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:14	I/O	I/O control output. Bit 15 Bit 14 Destination 0 0 Local 0 1 Remote 1 0 Mute 1 1 Both
13:12	HS	Handset output. Bit 13 Bit 12 Destination 0 0 Local 0 1 Remote 1 0 Mute 1 1 Both
11:10	L2DAC	Line 2 DAC output. Bit 15 Bit 14 Destination 0 0 Local 0 1 Remote 1 0 Mute 1 1 Both
9:8	PCM R/LF	PCM R/LF output. Bit 15 Bit 14 Destination 0 0 Local 0 1 Remote 1 0 Mute 1 1 Both
7:6	PCM CLS	PCM C,LS output. Bit 15 Bit 14 Destination 0 0 Local 0 1 Remote 1 0 Mute 1 1 Both
5:4	L1DAC	Line 1 DAC output. Bit 15 Bit 14 Destination 0 0 Local 0 1 Remote 1 0 Mute 1 1 Both
3:2	PCM L/R	PCM L/R output. Bit 15 Bit 14 Destination 0 0 Local 0 1 Remote 1 0 Mute 1 1 Both
1:0	CA	Command address output. Bit 15 Bit 14 Destination 0 0 Local 0 1 Remote 1 0 Reserved 1 1 Reserved

SDI Input Destination Control (Maestro2E_Base+3Ch, R/W)

I/O		HS		L2ADC		R		MIC ADC		L1ADC		PCM L/R		SA	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:14	I/O	I/O status input. Bit 15 Bit 14 Destination x 0 Local x 1 Remote
13:12	HS	Handset input. Bit 13 Bit 12 Destination 0 0 Local 0 1 Remote 1 x Mute both
11:10	L2ADC	Line 2 DAC input. Bit 15 Bit 14 Destination 0 0 Local 0 1 Remote 1 x Mute both
9:8	–	Reserved.
7:6	MIC ADC	MIC ADC input. Bit 15 Bit 14 Destination x 0 Local x 1 Remote
5:4	L1ADC	Line 1 ADC input. Bit 15 Bit 14 Destination 0 0 Local 0 1 Remote 1 x Mute both
3:2	PCM L/R	PCM L/R input. Bit 15 Bit 14 Destination 0 0 Local 0 1 Remote 1 0 Reserved 1 1 Both
1:0	SA	Status address/data input. Bit 15 Bit 14 Destination 0 0 Local 0 1 Remote 1 0 Reserved 1 1 Reserved

DAA Data Input / Output Port (Maestro2E_Base+50h,+51h, R/W)

DAA Data Input/Output															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	DDI/O	DAA data input/.output to AC'97 CODEC ext. 2.00.

GPIO Data (Maestro2E_Base+60h, +61h, R/W)

DS	PMES	HVS	GPIO data										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15	DS	Docking status. Read only.
14	PMES	PME# status. Read only.
13:12	HVS	Hardware volume control status from GD[7:6]. Read only.
11:0	GPD	GPIO data. Data input or output is controlled by the GPIO Direction register (Maestro2E_Base+68h, +69h). During input the data acts as a polarity control, combining with the external input signal to the internal circuits.

GPIO Mask (Maestro2E_Base+64h, +65h, R/W)

Reserved				GPIO write mask											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:12	–	Reserved.
11:0	GPWM	GPIO write mask. 1 = Mask write. 0 = Unmask write.

GPIO Direction (Maestro2E_Base+68h, +69h, R/W)

Reserved				GPIO direction											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:12	–	Reserved.
11:0	GPD	GPIO direction. 1 = Output. 0 = Input (default).

ASSP Memory / Index Port (Maestro2E_Base+80h,+81h, R/W)

ASSP memory/index															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	AM/I	Host-to-ASSP 16-bit memory index port. Points to 64K word of ASSP memory.

ASSP Memory Port (Maestro2E_Base+82h,+83h, R/W)

ADT	Reserved	MSS
15	14 13 12 11 10 9 8 7 6 5 4 3 2	1 0

Bit Definitions:

Bits	Name	Description
15	ADT	Aggressive DMA timing. 1 = Enable aggressive DMA timing. 0 = Disable aggressive DMA timing.
14:2	–	Reserved.
1:0	MSS	DMA memory space selection. Bit 1 Bit 0 Memory Space 0 x Reserved 1 0 ASSP program memory 1 1 ASSP data memory

ASSP Data Port (Maestro2E_Base+84h,+85h, R/W)

ASSP data
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Each time this register is accessed for a read or write, the ASSP Memory/Index port (Maestro2E_Base+80h, +81h) is incremented by 1. The index port is 4K word paged and consecutive access cannot cross this 4K word boundary.

Bit Definitions:

Bits	Name	Description
15:0	AD	16-bit data (word) port.

Game Port Address A (Maestro2E_Base+90h, R/W)

Native address port for game port
7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 200h.

Game Port Address B (Maestro2E_Base+91h, R/W)

Native address port for game port
7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 201h.

Game Port Address C (Maestro2E_Base+92h, R/W)

Native address port for game port
7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 202h.

Game Port Address D (Maestro2E_Base+93h, R/W)

Native address port for game port
7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 203h.

Game Port Address E (Maestro2E_Base+94h, R/W)

Native address port for game port
7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 204h.

Game Port Address F (Maestro2E_Base+95h, R/W)

Native address port for game port
7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 205h.

Game Port Address G (Maestro2E_Base+96h, R/W)

Native address port for game port
7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 206h.

Game Port Address H (Maestro2E_Base+97h, R/W)

Native address port for game port							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 207h.

MPU-401 Port Address A (Maestro2E_Base+98h, R/W)

Native address port for MPU-401							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAMPU	Native address port for MPU-401. Alias I/O port for 330h.

MPU-401 Port Address B (Maestro2E_Base+99h, R/W)

Native address port for MPU-401							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAMPU	Native address port for MPU-401. Alias I/O port for 331h.

MPU-401 Port Address C(Maestro2E_Base+9Ah, R/W)

Native address port for MPU-401							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAMPU	Native address port for MPU-401. Alias I/O port for 330h.

MPU-401 Port Address D(Maestro2E_Base+9Bh, R/W)

Native address port for MPU-401							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAMPU	Native address port for MPU-401. Alias I/O port for 331h.

Clock Multiplier Data Port A (Maestro2E_Base+9Ch, +9Dh, R)

R	7xS					4xS					3xS				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15	–	Reserved.
14:10	7xS	x7 counter status.
9:5	4xS	x4 counter status.
4:0	3xS	x3 counter status.

ASSP Control A (Maestro2E_Base+A2h, R/W)

43CLK	36CLK	Reserved	FPLU	33/49CLK	Reserved		0WS
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	43CLK	43 MHz DSP clock select. 1 = Select 43 Mhz DSP clock.
6	36CLK	36 MHz DSP clock select. 1 = Select 36 MHz DSP clock. **NOTE:** You must enable bits [31:30] (enable internal clock multiplier) before enabling this bit.
5	–	Reserved.
4	FPLU	Fast PLU enable. 1 = Enable fast PLU. 0 = Disable fast PLU.
3	33/49 CLK	33 MHz or 49 MHz ASSP clock select. 1 = Enable 49.152 MHz ASSP clock. 0 = Enable 33 MHz ASSP clock.
2:1	–	Reserved.
0	0WS	ASSP 0-wait state enable. 1 = Enable ASSP 0-wait state. 0 = Disable ASSP 0-wait state.

ASSP Control B (Maestro2E_Base+A4h, R/W)

Reserved			CRE	Reserved			ARST
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:5	–	Reserved.
4	CRE	Clock run/enable. 1 = Stop ASSP clock. 0 = Enable ASSP clock.
3:1	–	Reserved.
0	ARST	ASSP reset/run. 1 = Run ASSP. 0 = Reset ASSP.

ASSP Control C (Maestro2E_Base+A6h, R/W)

Reserved				HWP	Reserved	FM	AHI
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:4	–	Reserved.
3	HWP	Host write port enable. 1 = Enable host write port. 0 = Disable host write port.
2	–	Reserved.
1	FM	1 = Disable FM address remapping. 0 = Enable FM address remapping.
0	AHI	ASSP-to-host interrupt request enable. 1 = Enable ASSP-to-host interrupt request. 0 = Disable ASSP-to-host interrupt request.

Host Write Index (Maestro2E_Base+A8h, R/W)

HWIR[7:0]							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	HWIR[7:0]	Host write index register.

Host Write Data (Maestro2E_Base+AAh, R/W)

HWDR[7:0]							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	HWDR[7:0]	Host write data register. An interrupt to ASSP is generated when the host writes this data port.

ASSP to Host Interrupt Request Status (Maestro2E_Base+ACh, R/W)

ASSP IRQ status							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	AIS	ASSP to host software interrupt request status. Read for pending interrupt status. 1 = Interrupt pending. 0 = No interrupt pending. Write 1 to clear pending interrupt request. The bits in this register are set to 1 by ASSP to request interrupts from the host. A read checks the status of the interrupt. Writing 1 clears a pending request by the host only.

ES978 Miscellaneous Control (Maestro2E_Base+C0h, R/W)

MIDI TX S	MIDI LB	MOE	RSS			AI	
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	MIDI TX S	MIDI transmit signal.
6	MIDI LB	MIDI loopback test.
5	MOE	Master output enable.
4:2	RSS	Record source select. Bit 4 / Bit 3 / Bit 2 / Record Source x / 0 / x / Microphone 0 / 1 / x / Aux A (CD) input 1 / 1 / 0 / Line input 1 / 1 / 1 / Mixer
1:0	AI	Mode of expansion analog interface. Read-only by host; write by logic. Bit 1 / Bit 0 / Mode 0 / 0 / 0 0 / 1 / 1 1 / 0 / 2 1 / 1 / 3

MIDI Transmit Data (Maestro2E_Base+C1h, R/W)

MIDI transmit data							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	MIDI TX D	MIDI transmit data. Read-only by host; write by logic.

XGPO Data (Maestro2E_Base+C2h, R/W)

XGPO data							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	XGPO D	XGPO data.

Playback Mixer – Host Audio Volume (Maestro2E_Base+C3h, R/W)

Playback host audio volume left				Playback host audio volume right			
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:4	PHAVL	Playback mixer – host audio volume left.
3:0	PHAVR	Playback mixer – host audio volume right.

Playback Mixer – Line Volume (Maestro2E_Base+C4h, R/W)

Playback line volume left				Playback line volume right			
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:4	PLVL	Playback mixer – line volume left.
3:0	PLVR	Playback mixer – line volume right.

Playback Mixer – Mic Volume (Maestro2E_Base+C5h, R/W)

Playback mic volume left				Playback mic volume right			
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:4	PMVL	Playback mixer – mic volume left.
3:0	PMVR	Playback mixer – mic volume right.

Playback Mixer – Aux A (CD) Volume (Maestro2E_Base+C6h, R/W)

Playback aux A (CD) volume left				Playback aux A (CD) volume right			
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:4	PCDVL	Playback mixer – Aux A (CD) volume left.
3:0	PCDVR	Playback mixer – Aux A (CD) volume right.

Playback Mixer – Aux B Volume (Maestro2E_Base+C7h, R/W)

Playback aux B volume left				Playback aux B volume right			
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:4	PABVL	Playback mixer – Aux B volume left.
3:0	PABVR	Playback mixer – Aux B volume right.

Playback Mixer – I²S/ES689/ES69x Volume (Maestro2E_Base+C8h, R/W)

Playback I²S/ES689/ES69x vol left				Playback I²S/ES689/ES69x vol right			
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:4	PI²SVL	Playback mixer – I²S/ES689/ES69x volume left.
3:0	PI²SVR	Playback mixer – I²S/ES689/ES69x volume right.

Record Mixer – Record Volume (Maestro2E_Base+C9h, R/W)

Record volume left				Record volume right			
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:4	RVL	Record mixer – record volume left.
3:0	RVR	Record mixer – record volume right.

Record Mixer – Line Volume (Maestro2E_Base+CAh, R/W)

Record line volume left				Record line volume right			
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:4	RLVL	Record mixer – line volume left.
3:0	RLVR	Record mixer – line volume right.

Record Mixer – Mic Volume (Maestro2E_Base+CBh, R/W)

Record mic volume left				Record mic volume right			
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:4	RMVL	Record mixer – mic volume left.
3:0	RMVR	Record mixer – mic volume right.

Record Mixer – Aux A (CD) Volume (Maestro2E_Base+CCh, R/W)

Record aux A (CD) volume left				Record aux A (CD) volume right			
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:4	RCDVL	Record mixer – Aux A (CD) volume left.
3:0	RCDVR	Record mixer – Aux A (CD) volume right.

Record Mixer – Aux B Volume (Maestro2E_Base+CDh, R/W)

Record aux B volume left				Record aux B volume right			
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:4	RABVL	Record mixer – Aux B volume left.
3:0	RABVR	Record mixer – Aux B volume right.

Record Mixer – I²S/ES689/ES69x Volume (Maestro2E_Base+CEh, R/W)

Record I²S/ES689/ES69x vol left				Record I²S/ES689/ES69x vol right			
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:4	RI²SVL	Record mixer – I²S/ES689/ES69x volume left.
3:0	RI²SVR	Record mixer – I²S/ES689/ES69x volume right.

Master Volume Left (Maestro2E_Base+CFh, R/W)

x	Mute left	Master volume left					
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	–	No function.
6	ML	Mute left. 1 = mute.
5:0	MVL	Master volume left.

Master Volume Right (Maestro2E_Base+D0h, R/W)

x	Mute right	Master volume right					
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	–	No function.
6	MR	Mute right. 1 = mute.
5:0	MVR	Master volume right.

CRC Checksum (Maestro2E_Base+D1h, R/W)

CRC checksum							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	CRCC	CRC checksum. Read-only by host; write by logic.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Ratings	Symbol	Value	Units
DC power voltage	VDD	-0.3 to VDD+0.3	V
Input voltage	VIN	-0.3 to VDD+0.3	V
Operating temperature range	TO	0 to 70	Deg C
Storage temperature range	TST	-40 to 125	Deg C
Maximum power dissipation at TJ = 125 °C	PDMAX	300	mW

WARNING: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

Operating Conditions

DVdd	3.3 V ± 5%
TA	25°
External Load	50 pF

Table 15 Digital Characteristics

Parameter	Symbol	Min	Typ	Max	Unit (conditions)
Input low voltage: all except clock pins (XTALI)	VIL	0.4	–	2.4	V
Input high voltage: all except clock pins (XTALI)	VIH	2.0	–	DVdd + 0.5	V
Output high voltage	VOH	2.4	–	DVdd	V
Output low voltage	VOL	0.0	0.2	0.4	V
Input leakage current: all except pull-up/pull-down pins	–	-10	–	10	µA
Output leakage current: all except pull-up/pull-down pins	–	-10	–	10	µA
Output buffer drive current	–	–	5	–	mA

POWER MANAGEMENT CHARACTERISTICS

Table 16 Current Consumption

Operating Mode	Typical IDDD at 3.3 V	Power Consumption: (IDDD x 3.3 V) Watt
Full power-on (nothing powered down) at 33 MHz	100 mA	0.330 W

TIMING SPECIFICATIONS

AC-Link Timing Specifications

AC-Link Timing Diagrams

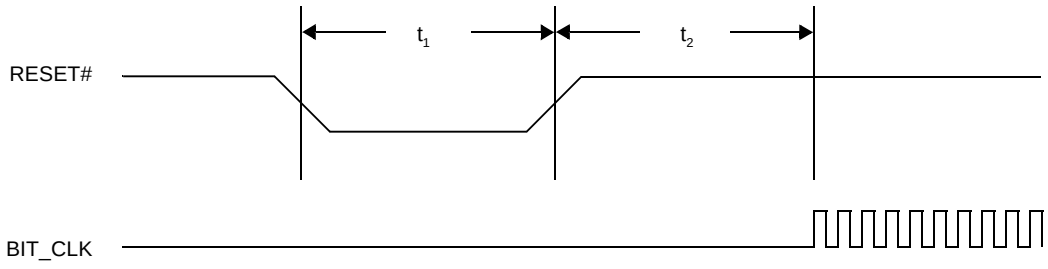


Figure 11 Cold Reset

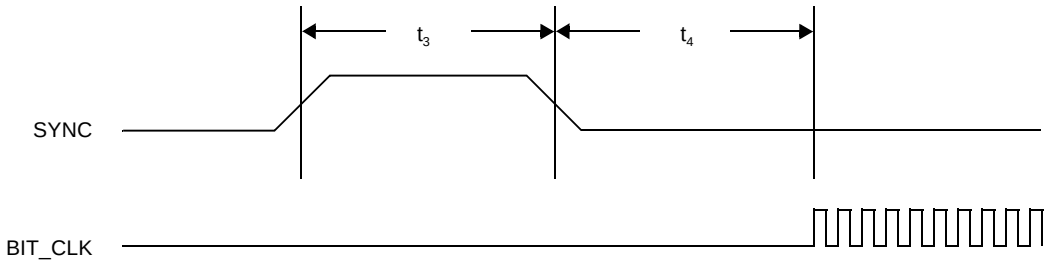


Figure 12 Warm Reset

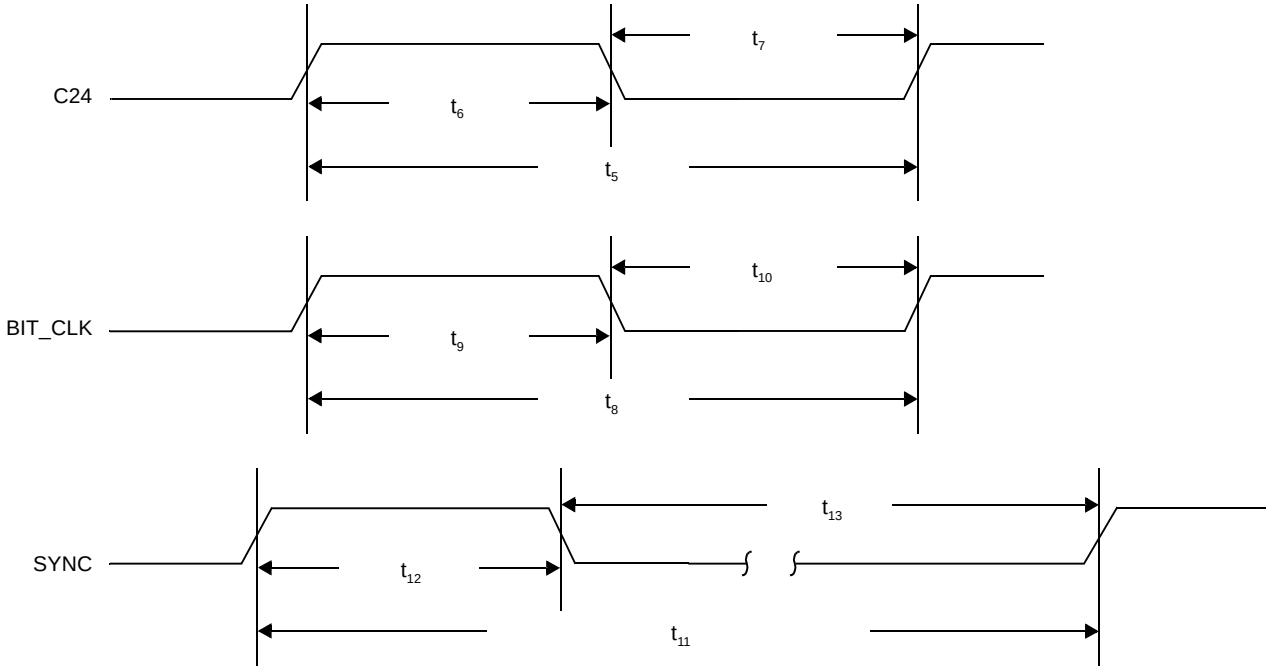


Figure 13 Clocks

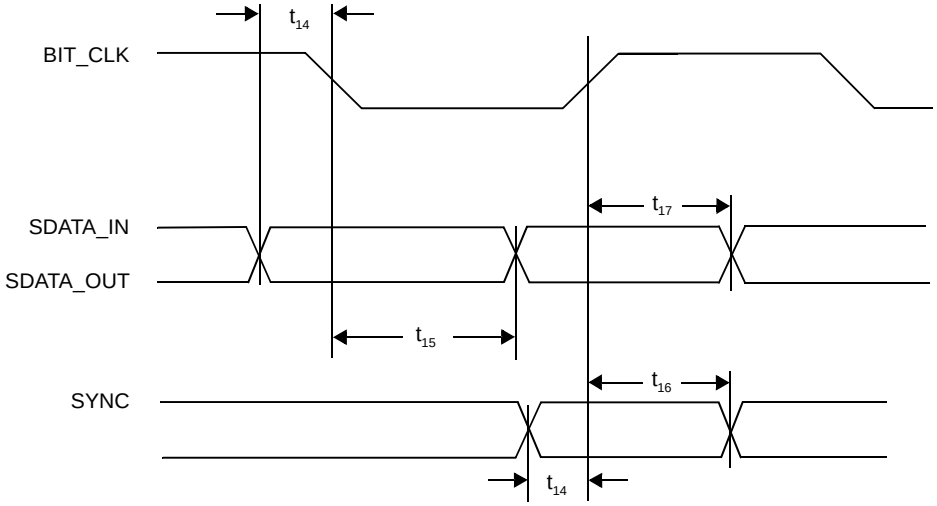


Figure 14 Data Setup and Hold

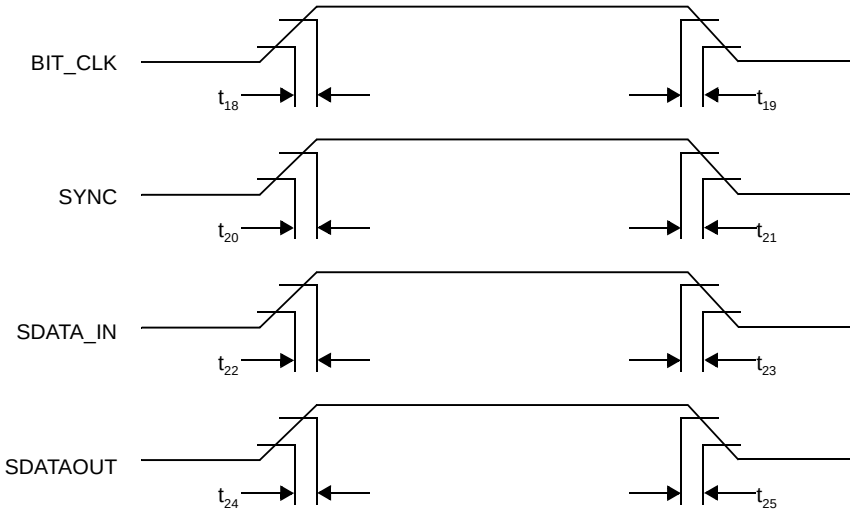
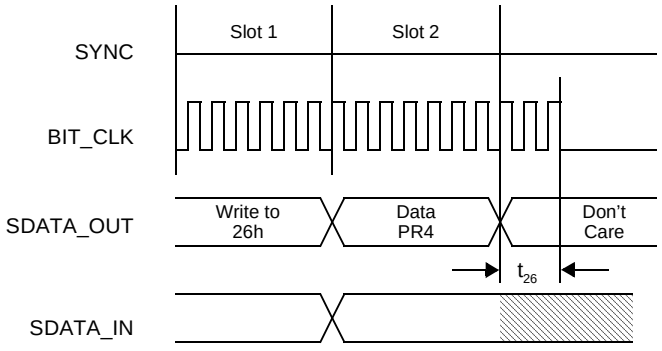


Figure 15 Signal Rise and Fall Times



Note: BIT_CLK not to scale.

Figure 16 AC-Link Low Power Mode Timing

AC-Link Timing Characteristics

Table 17 AC-Link Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_1	RESET# active-low pulse width	1.0			µS
t_2	RESET# inactive to BIT_CLK start-up delay	162.8			nS
t_3	SYNC active-high pulse width		1.3		µS
t_4	SYNC inactive to BIT_CLK start-up delay	162.8			nS
	C24 frequency		25.0		MHz
t_5	C24 period		40.0		nS
t_6	C24 high pulse width	20.41	20.72	21.03	nS
t_7	C24 low pulse width	18.97	19.28	19.59	nS
	BIT_CLK frequency		12.5		MHz
t_8	BIT_CLK period		80.0		nS
t_9	BIT_CLK high pulse width	32.0	40.0	48.0	nS
t_{10}	BIT_CLK low pulse width	32.0	40.0	48.0	nS
	SYNC frequency		48.8		KHz
t_{11}	SYNC period		20.49		µS
t_{12}	SYNC high pulse width		1.28		µS
t_{13}	SYNC low pulse width		19.21		µS
t_{14}	Setup to falling edge of BIT_CLK	15.0			nS
t_{15}	Hold from falling edge of BIT_CLK	5.0			nS
t_{16}	Valid delay from BIT_CLK rising edge	4		10	nS
t_{17}	Valid delay from BIT_CLK rising edge	4		10	nS
t_{18}	BIT_CLK rise time	2		6	nS
t_{19}	BIT_CLK fall time	2		6	nS
t_{20}	SYNC rise time	2		6	nS
t_{21}	SYNC fall time	2		6	nS
t_{22}	SDATA_IN rise time	2		6	nS
t_{23}	SDATA_IN fall time	2		6	nS
t_{24}	SDATA_OUT rise time	2		6	nS
t_{25}	SDATA_OUT fall time	2		6	nS
t_{26}	End of Slot 2 to BIT_CLK, SDATA_IN low			1.0	µS

PCI Bus Timing Specifications

PCI Bus Timing Diagrams

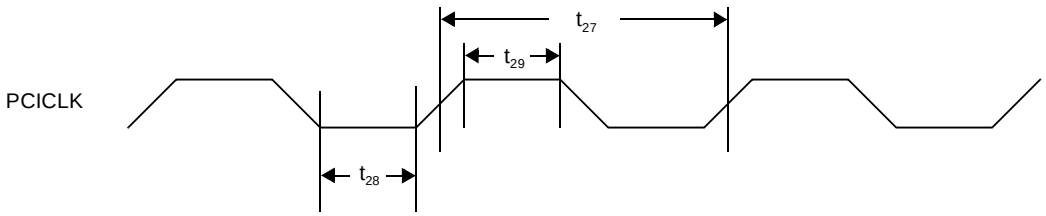


Figure 17 PCI Clock Timing

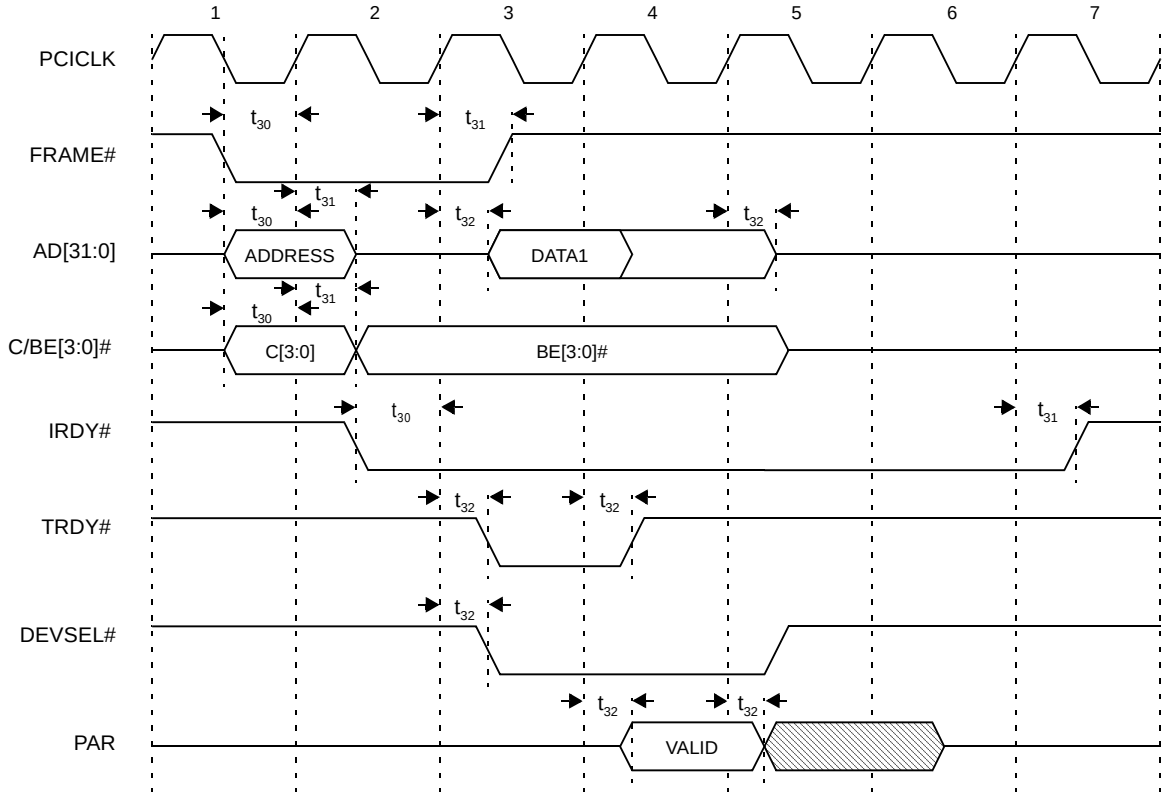


Figure 18 PCI Bus I/O Read Cycle

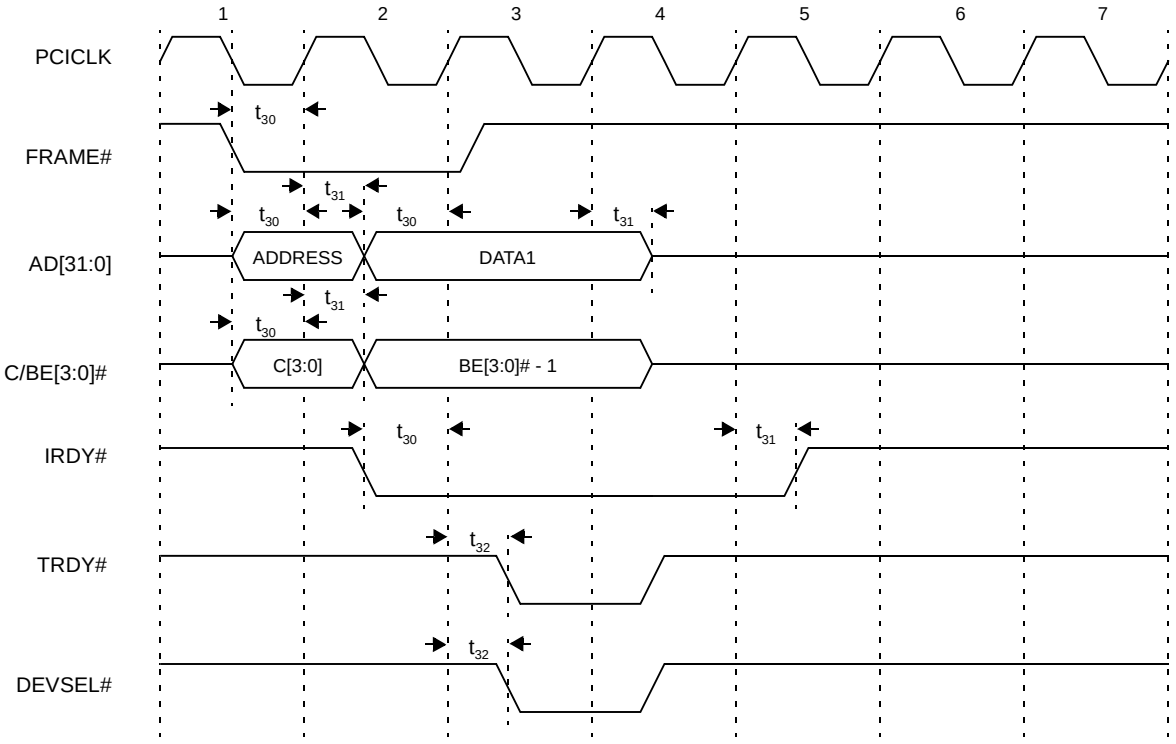


Figure 19 PCI Bus I/O Write Cycle

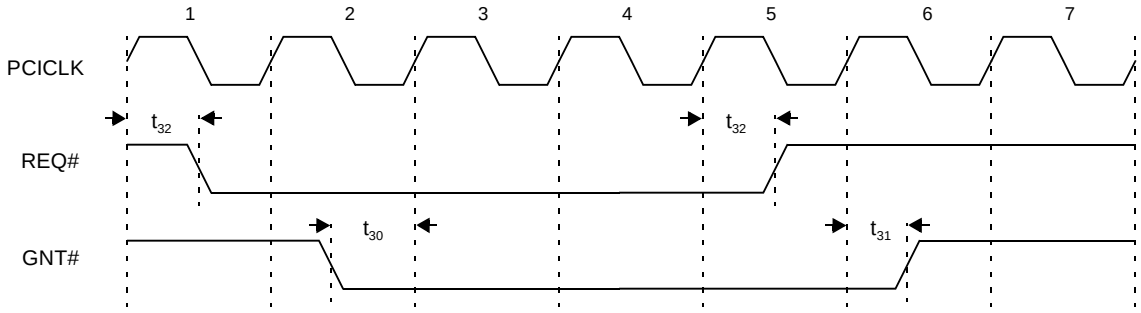


Figure 20 PCI Bus Master Request

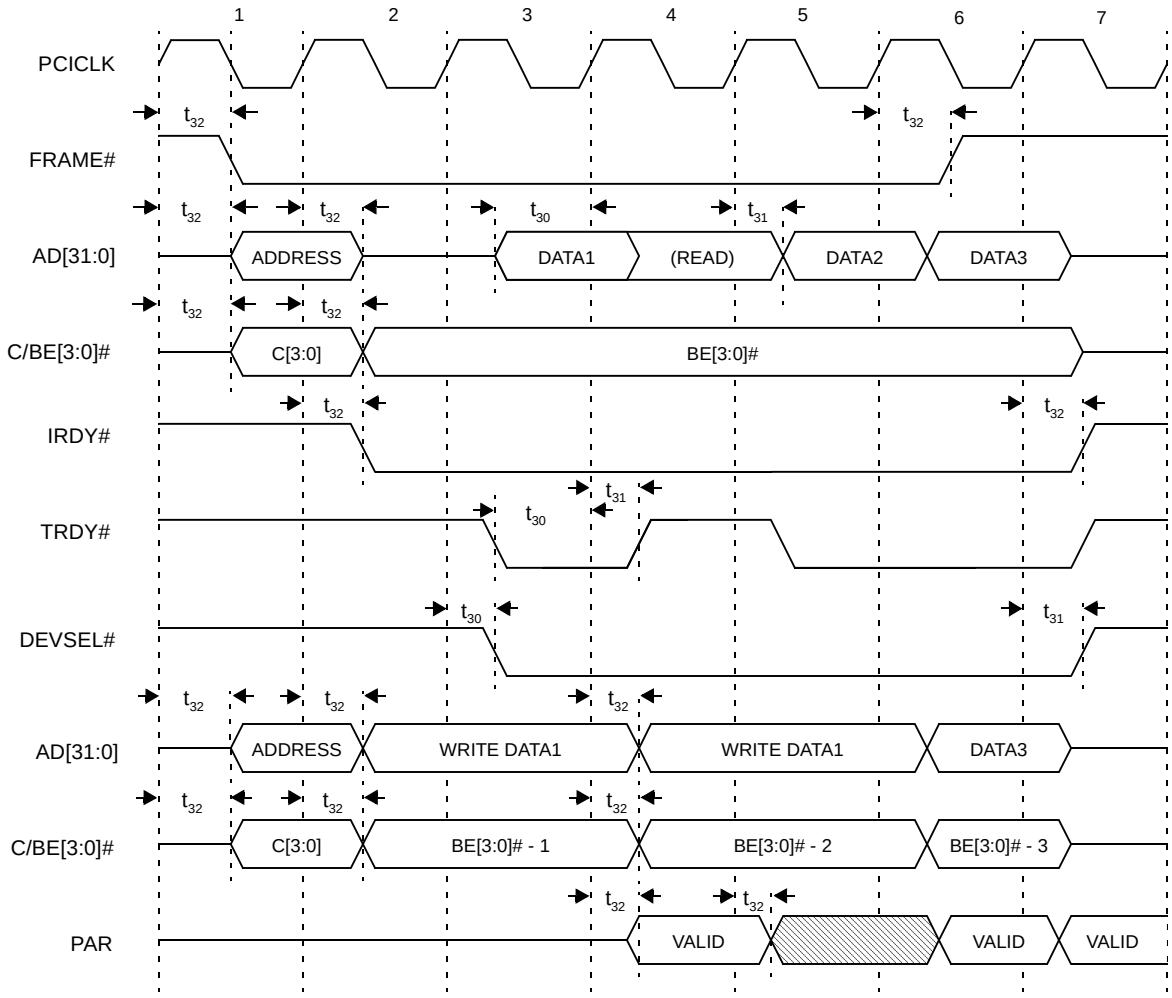


Figure 21 PCI Bus Master Read/Write Cycle

PCI Bus Timing Characteristics

Table 18 PCI Bus Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Units (Conditions)
t_{27}	PCI bus clock cycle time	30			nS
t_{28}	PCI bus clock low pulse width	11			nS
t_{29}	PCI bus clock high pulse width	11			nS
t_{30}	Input setup time to PCICLK	7			nS
t_{31}	Input hold time to PCICLK	0			nS
t_{32}	Output propagation delay Time from PCICLK	2		11	nS (0 pF load) (50 pF load)

I²S Port Timing Specifications

I²S Port Timing Diagram

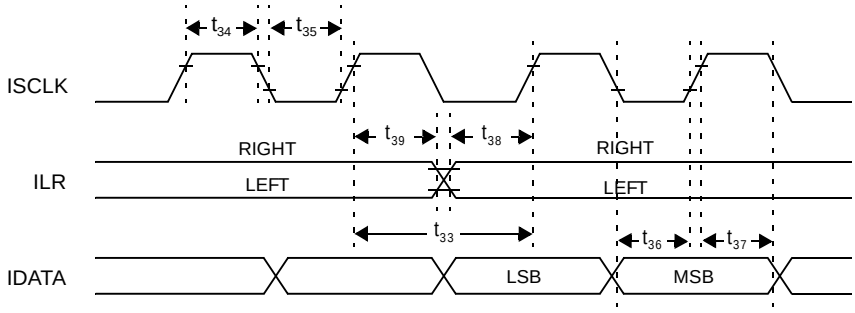


Figure 22 I²S Port Timing

I²S Port Timing Characteristics

Table 19 I²S Port Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{33}	ISCLK cycle time	54			nS
t_{34}	ISCLK HIGH time	15			nS
t_{35}	ISCLK LOW time	15			nS
t_{36}	IDATA setup time	12			nS
t_{37}	IDATA hold time	2			nS
t_{38}	ILR setup time	12			nS
t_{39}	ILR hold time	2			nS

ES978 Docking Interface Timing Specifications

ES978 Docking Interface Timing Diagram

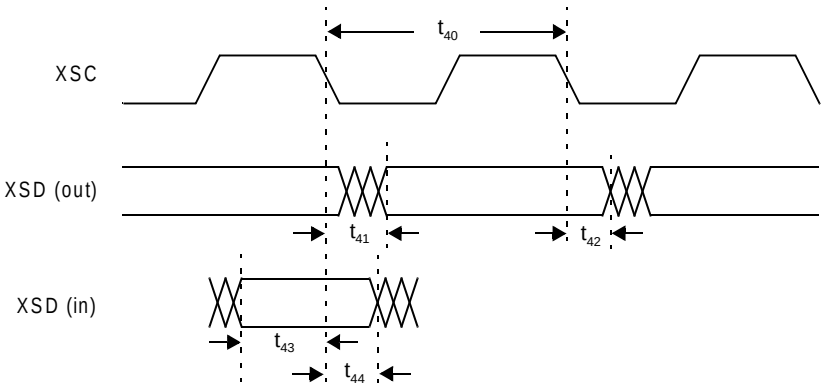


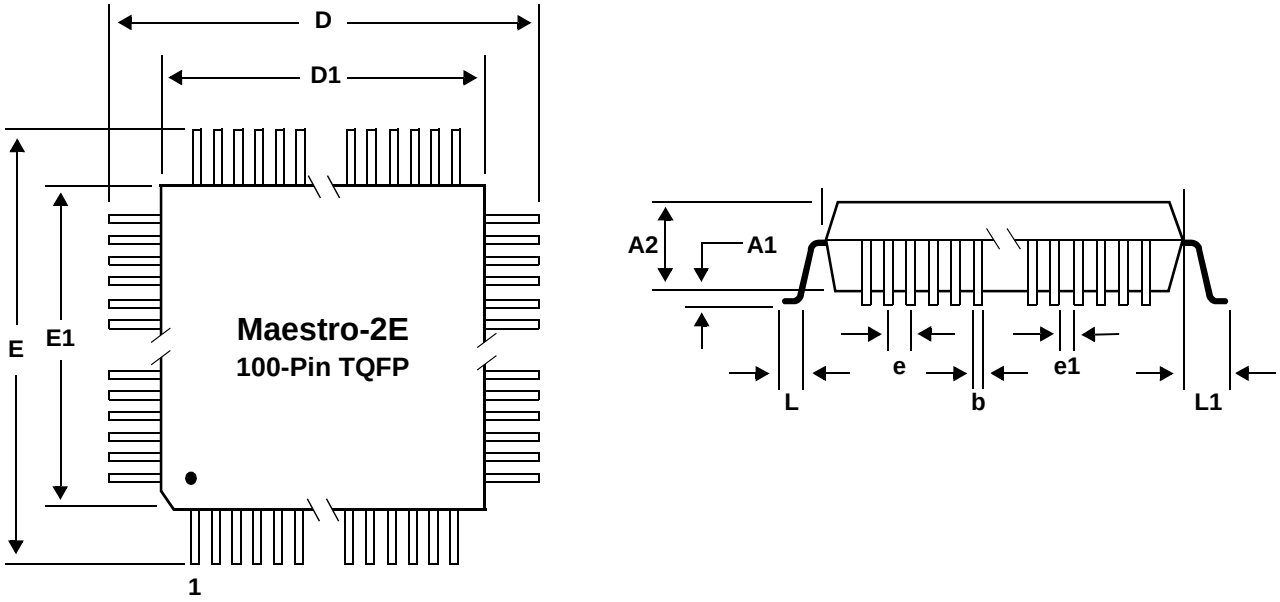
Figure 23 ES978 Docking Interface Timing

ES978 Docking Interface Timing Characteristics

Table 20 ES978 Docking Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{40}	XSC period		$f_{XTAL}/4$		nS (Duty: 40 to 60%)
t_{41}	XSD output delay			15	nS
t_{42}	XSD output hold	0			nS
t_{43}	XSD input setup	10			nS
t_{44}	XSD input hold	0			nS

MECHANICAL DIMENSIONS



Symbol	Description	Millimeters		
		Min	Nom	Max
D	Lead to lead, X-axis	15.75	16.00	16.25
D1	Package's outside, X-axis	13.90	14.00	14.10
E	Lead to lead, Y-axis	15.75	16.00	16.25
E1	Package's outside, Y-axis	13.90	14.00	14.10
A1	Board standoff	0.05	0.10	0.15
A2	Package thickness	1.35	1.40	1.45
b	Lead width	0.17	0.22	0.27
e	Lead pitch	-	0.50	-
e1	Lead gap	0.24	-	-
L	Foot length	0.45	0.60	0.75
L1	Lead length	0.93	1.00	1.07
-	Foot angle	0°		7°
-	Coplanarity	-	-	0.102
-	Leads in X-axis	-	25	-
-	Leads in Y-axis	-	25	-
-	Total leads	-	100	-
-	Package type	-	TQFP	-

Figure 24 Maestro-2E Mechanical Dimensions

APPENDIX A: SCHEMATIC EXAMPLES

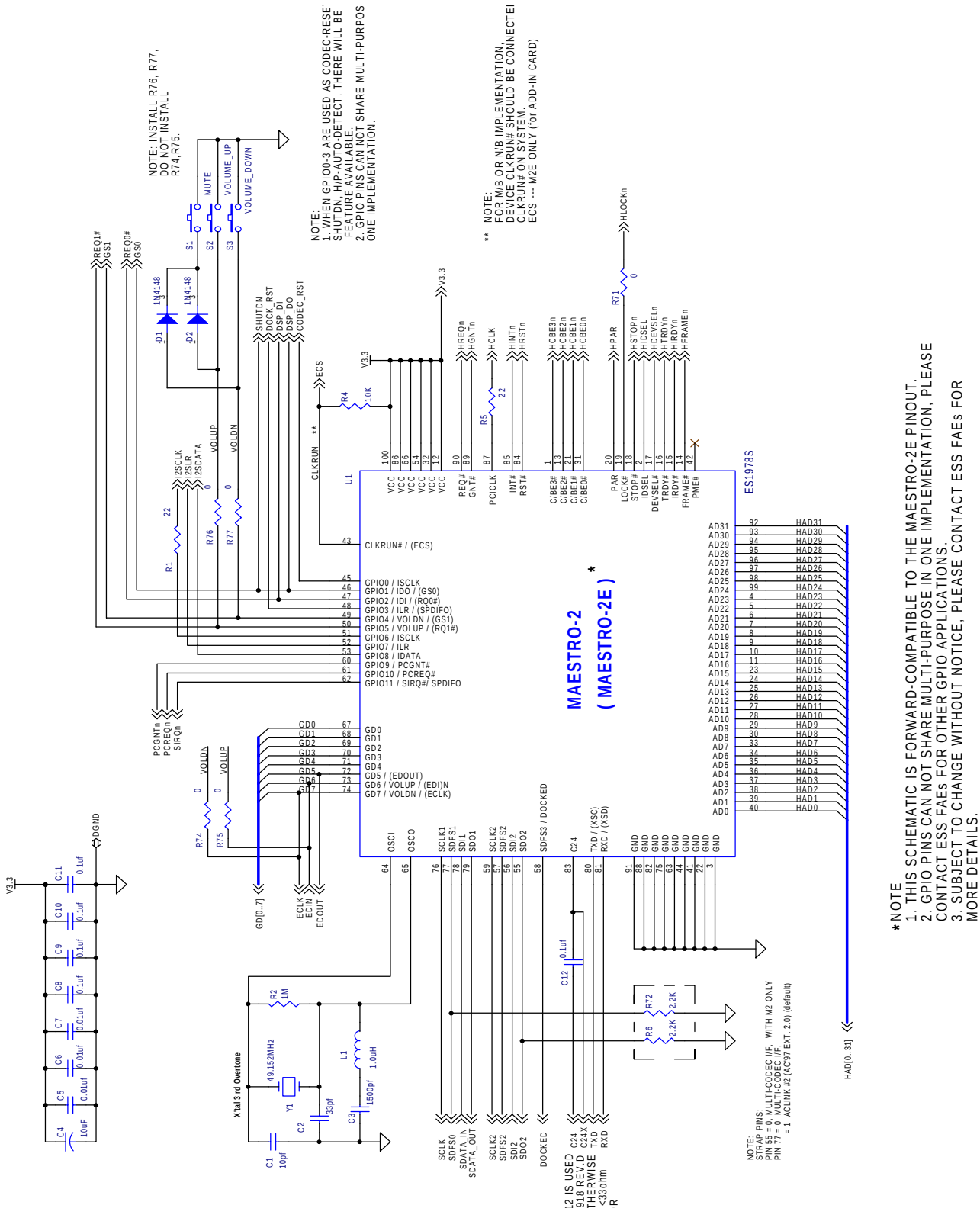


Figure 25 Maestro-2E

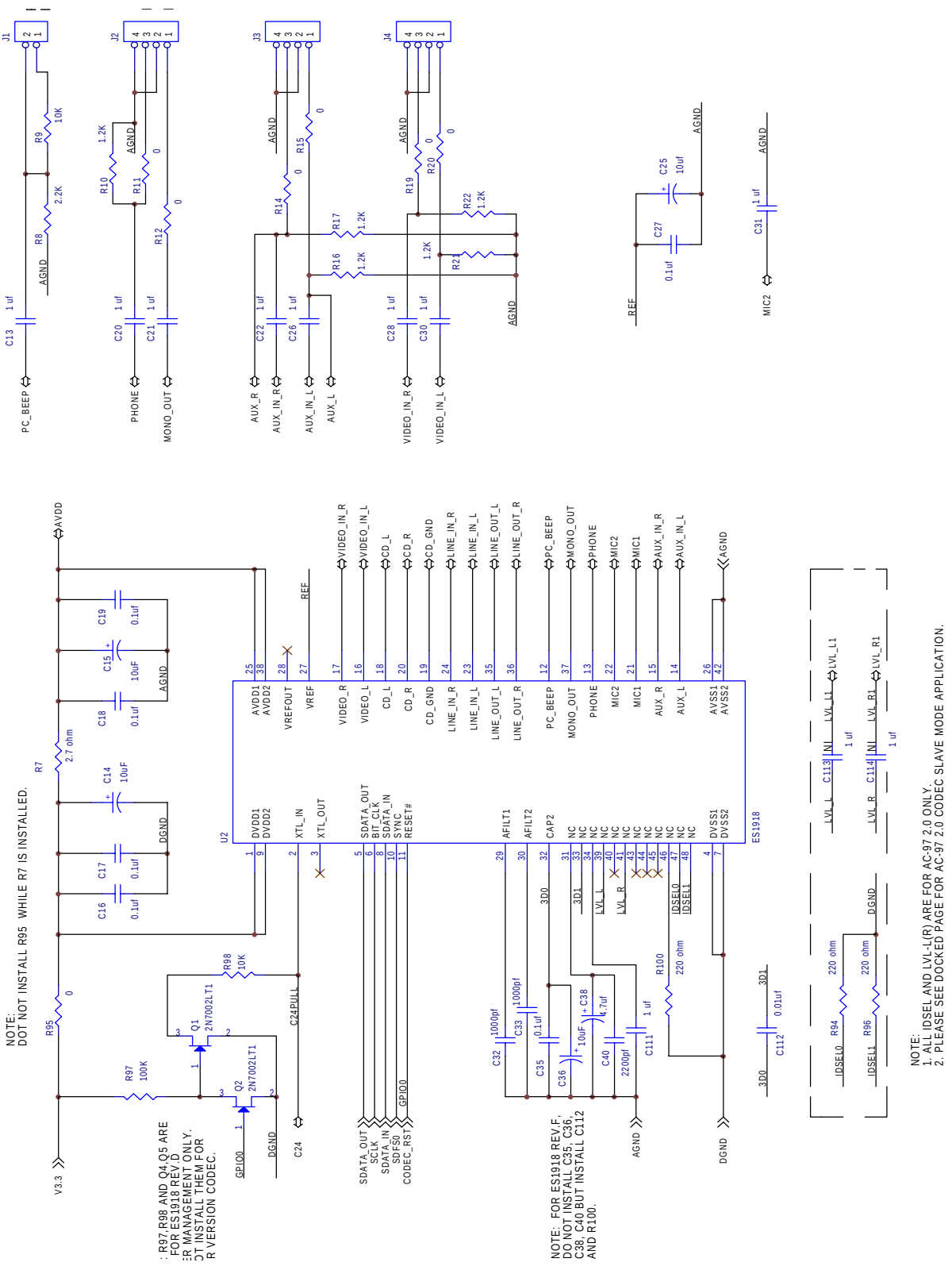


Figure 26 CODEC Interface

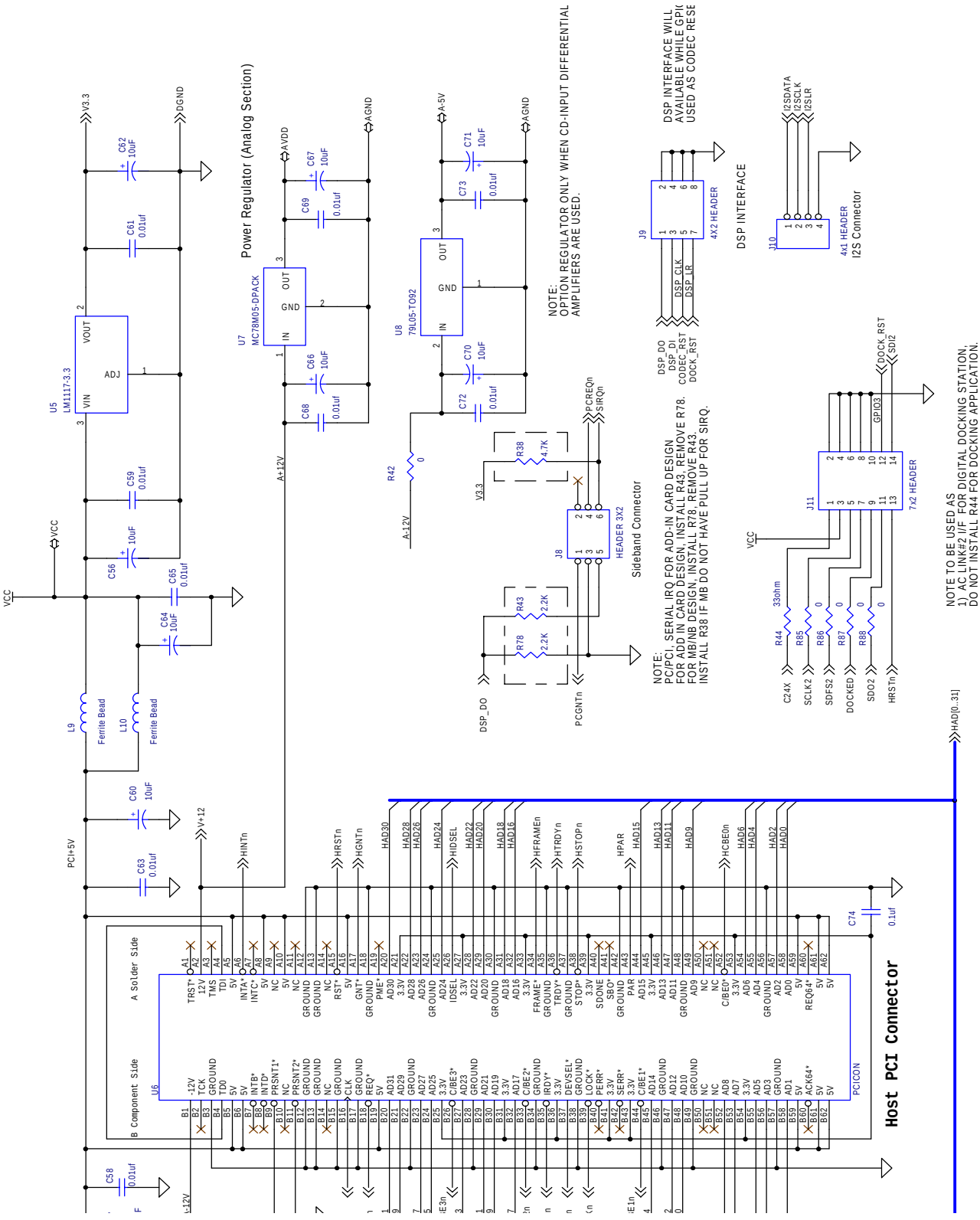


Figure 27 Host PCI Interface

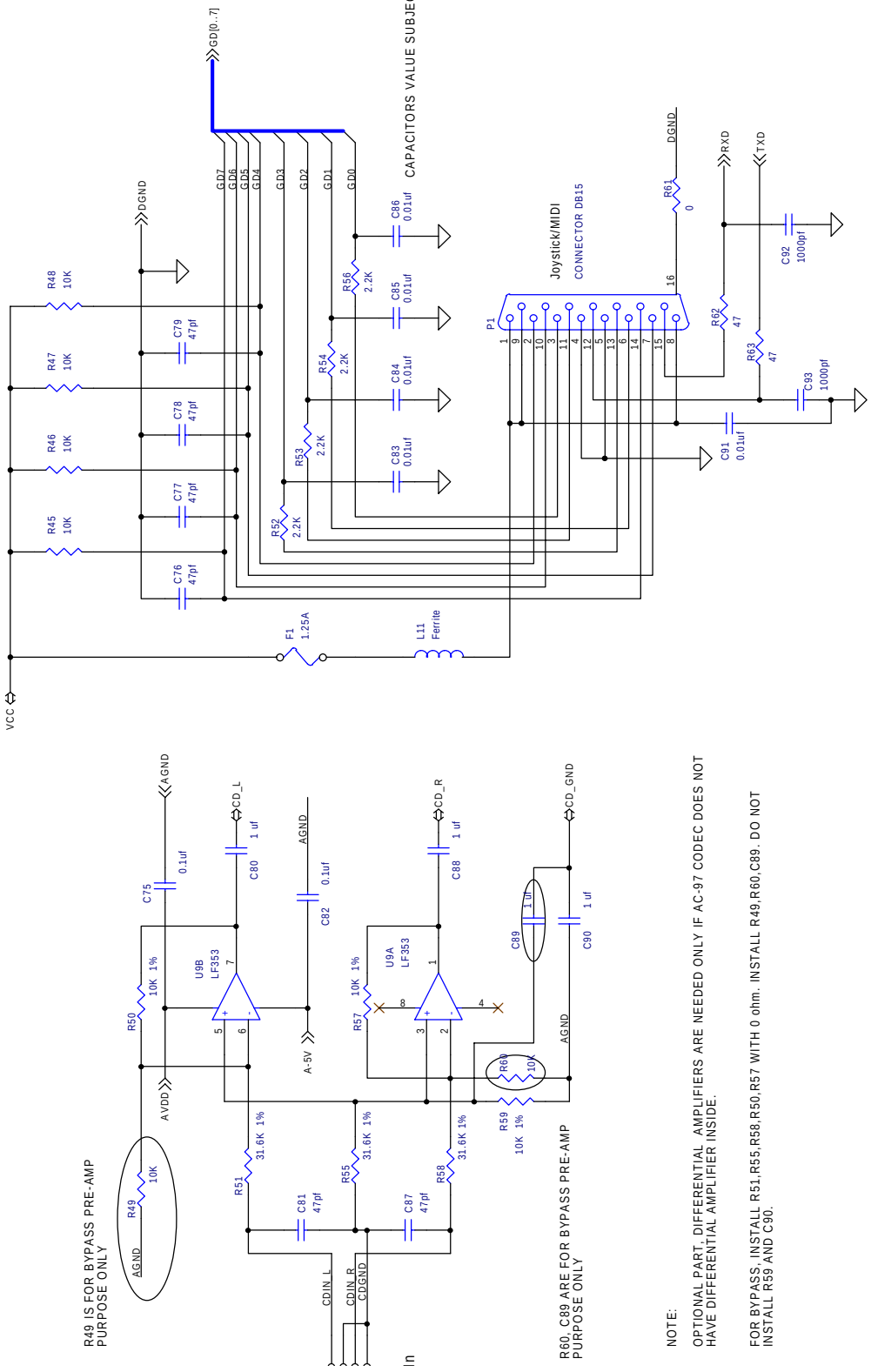


Figure 28 CD/MIDI Section

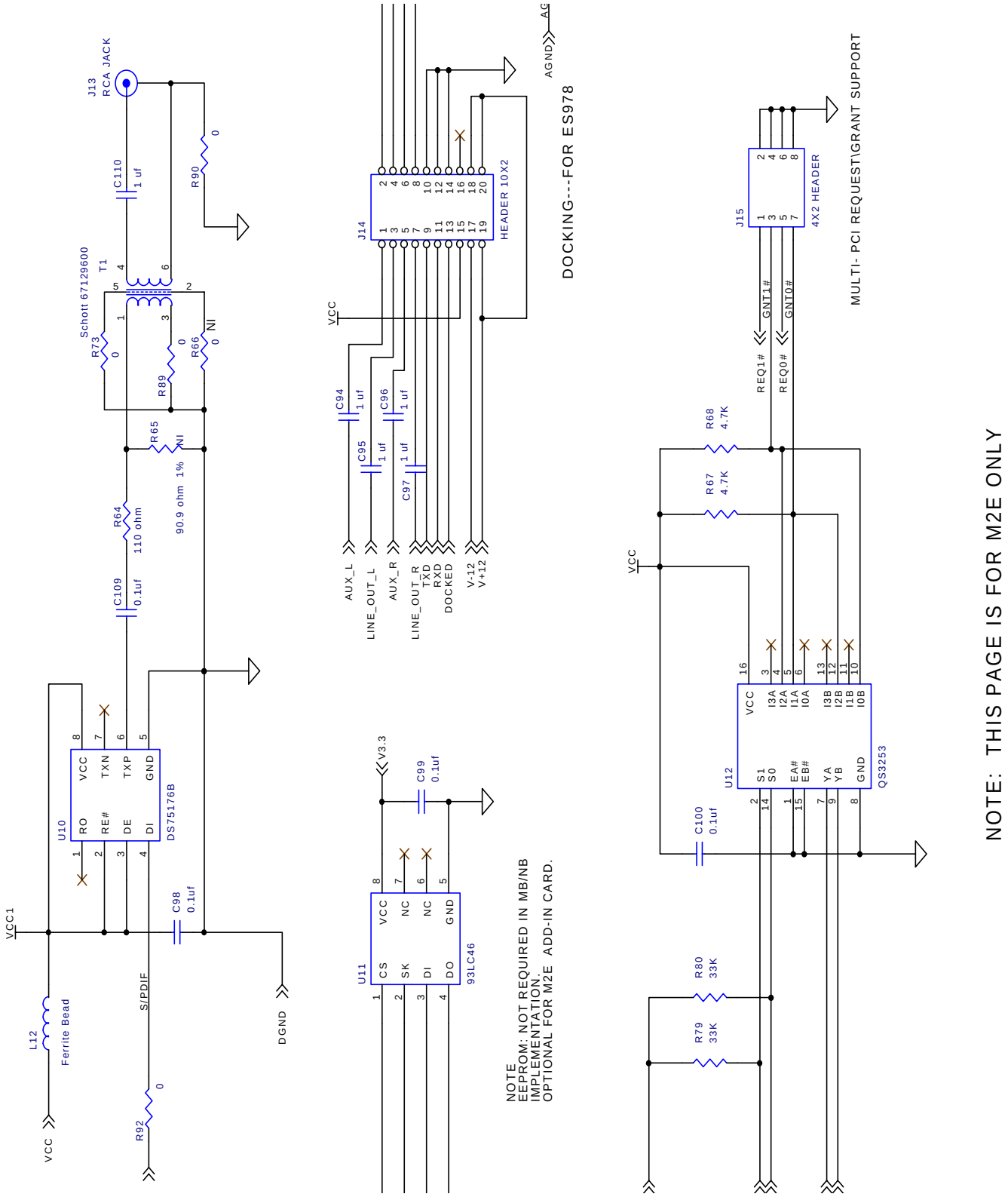


Figure 29 Maestro-2E Miscellaneous Sections

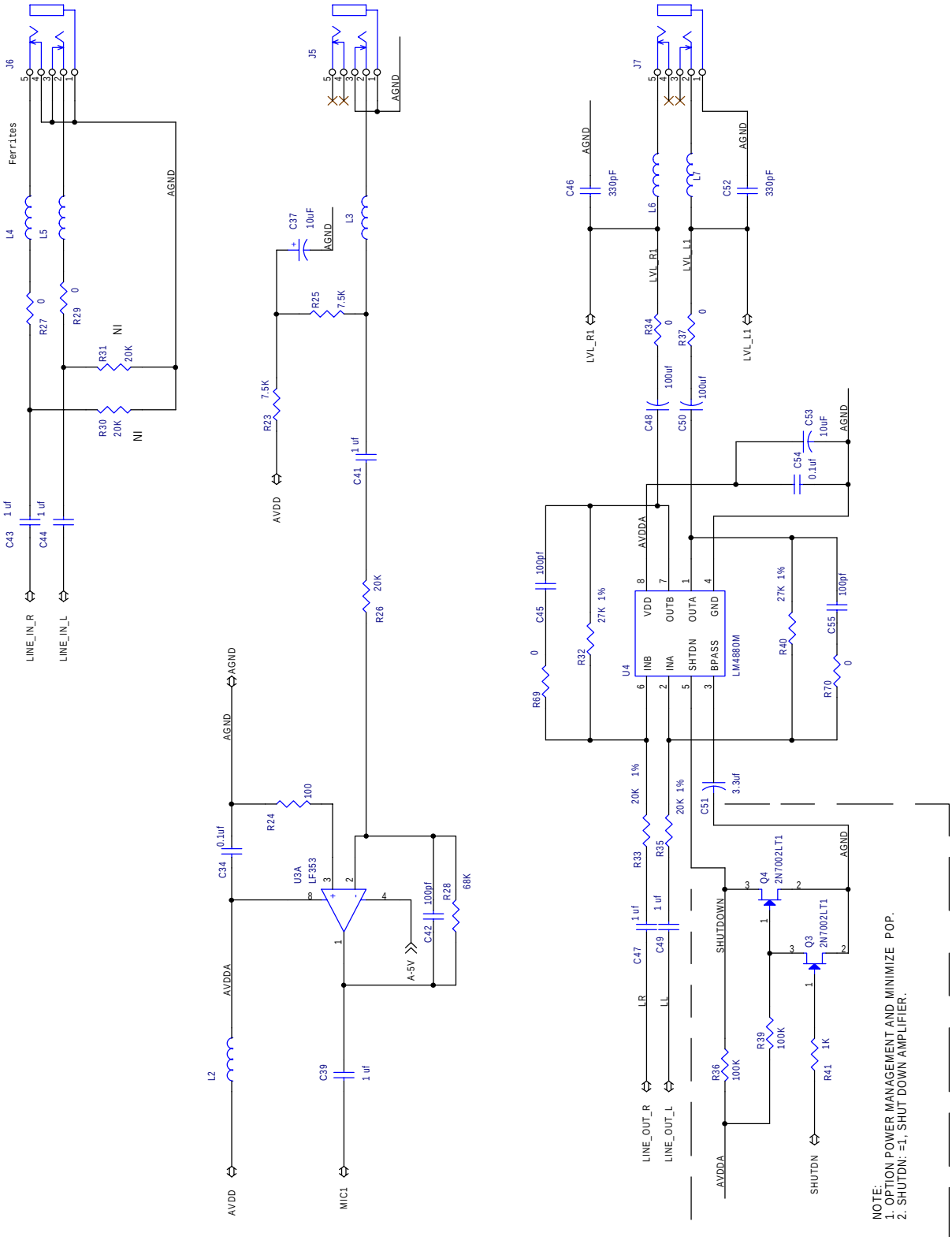


Figure 30 Amplifier Section

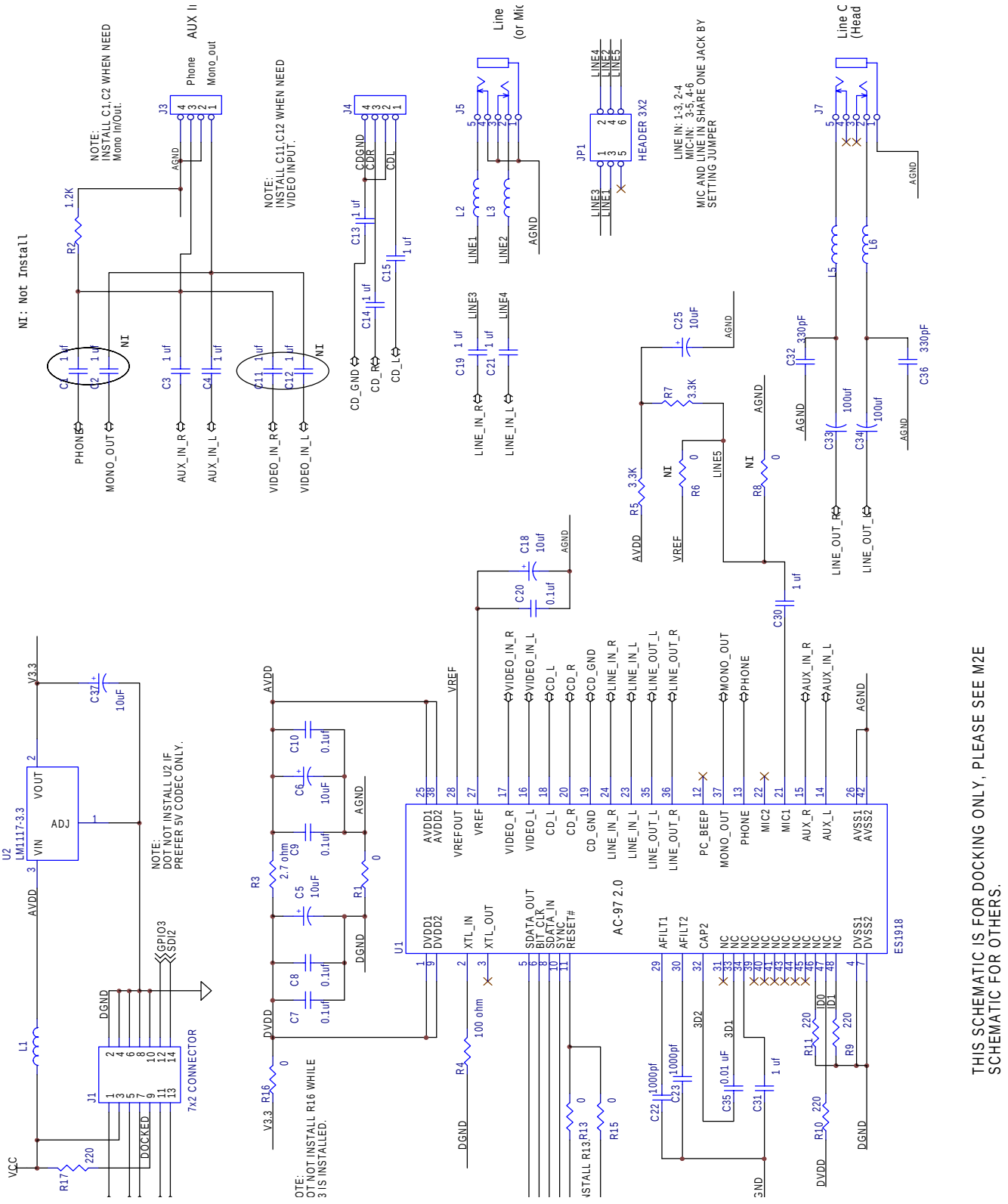


Figure 31 Docking Interface

APPENDIX B: BILL OF MATERIALS

Table 21 Bill of Materials (BOM)

Item	Quantity	Reference	Part
1	1	C1	10 pF
2	1	C2	33 pF
3	1	C3	1500 pF
4	16	C4,C14,C15,C25,C36,C37,C53,C56,C57,C60,C62,C64,C66,C67,C70,C71	10 µF
5	18	C5,C6,C7,C58,C59,C61,C63,C65,C68,C69,C72,C73,C83,C84,C85,C86, C91,C112	0.01 µF
6	20	C8,C9,C10,C11,C12,C16,C17,C18,C19,C27,C34,C35,C54,C74,C75,C82, C98,C99,C100,C109	0.1 µF
7	26	C13,C20,C21,C22,C26,C28,C30,C31,C39,C41,C43,C44,C47,C49,C80, C88,C89,C90,C94,C95,C96,C97,C110,C111,C113,C114	1 µF
8	4	C32,C32,C92,C93	1000 pF
9	1	C38	4.7 µF
10	1	C40	2200 pF
11	3	C42,C45,C55	100 pF
12	2	C52,C46	330 pF
13	2	C48,C50	100 µF
14	1	C51	3.3 µF
15	6	C76,C77,C78,C79,C81,C97	47 pF
16	2	D1,D2	1N4148
17	1	F1	1.25 A
18	1	J1	HEADER 2x1
19	4	J2,J3,J4,J12	HEADER 4x1
20	3	J5,J6,J7	PHONEJACK STEREO
21	1	J8	HEADER 3x2
22	2	J9,J15	HEADER 4x2
23	1	J10	HEADER 4x1
24	1	J11	HEADER 7x2
25	1	J13	RCA Jack
26	1	J14	HEADER 10x2
27	1	L1	1.0 µH
28	9	L2,L3,L4,L5,L6,L7,L9,L10,L12	FERRITE BEAD
29	1	L11	FERRITE BEAD
30	1	P1	CONNECTOR DB15
31	4	Q1,Q2,Q3,Q4	2N7002LT1
32	2	R1,R5	22 ohm
33	1	R2	1M
34	9	R4,R9,R45,R46,R47,R48,R49,R60,R98	10K
35	9	R6,R8,R43,R52,R53,R54,R56,R72,R78	2.2K
36	1	R7	2.7 ohm
37	5	R10,R16,R17,R21,R22	1.2K

Table 21 Bill of Materials (BOM) (Continued)

Item	Quantity	Reference	Part
38	32	R11,R12,R14,R15,R19,R20,R27,R29,R34,R37,R42,R61,R66,R69,R70, R71,R73,R74,R75,R76,R77,R85,R86,R87,R88,R89,R90,R92,R94,R95, R96,R99	0 ohm
39	2	R23,R25	7.5K
40	1	R24	100 ohm
41	3	R26,R30,R31	20K
42	1	R28	68K
43	2	R32,R40	27K, 1%
44	2	R33,R35	20K, 1%
45	3	R36,R39,R97	100K
46	3	R38,R67,R68	4.7K
47	1	R41	1K
48	1	R44	33 ohm
49	3	R50,R57,R59	10K, 1%
50	3	R51,R55,R58	31.6K, 1%
51	2	R63,R62	47 ohm
52	1	R64	110 ohm
53	2	R79,R80	33K
54	1	S1,S2,S3	PUSHBUTTON
55	1	T1	Schott 67129600
56	1	U1	ES1978S
57	1	U2	ES1918
58	2	U3,U9	LF353
59	1	U4	LM4880M
60	1	U5	LM1117-3.3
61	1	U6	PCICON
62	1	U7	MC78M05-DPACK
63	1	U8	79L05-TO92
64	1	U10	DS75176B
65	1	U11	93LC46
66	1	U12	QS3253
67	1	Y1	49.152 MHz

ESS Technology, Inc.
48401 Fremont Blvd.
Fremont, CA 94538
Tel: 510-492-1088
Fax: 510-492-1098