DESCRIPTION

The ES1983 Maestro-3i^TM PCI audio-modem accelerator combines advanced audio and modem functionality in a highly integrated PCI solution for notebook systems. It uses the high-bandwidth PCI bus to deliver advanced PC audio features, such as HRTF 3-D positional audio, DirectSound acceleration and DVD AC-3 5.1 to 2 speaker virtualization.

The ES1983 provides a high-quality docking solution using either the secondary AC'97 Extension 2.1 compliant interface or the secondary I^{2}S interface. In addition, the ES1983 includes S/PDIF input support for PCM digital audio contents.

The ES1983 implements multi-stream DirectSound and DirectSound3D acceleration with digital mixing, sample rate conversion and HRTF 3-D filtering. The ES1983 maintains full DOS legacy audio compatibility over the standard PCI 2.1 and PCI 2.2 buses. The ES1983 is designed for high-performance consumer multimedia notebook PC applications.

The ES1983 includes a programmable audio signal processor and provides simultaneous support for multiple audio streams. With its built-in DSP core, the ES1983 uses its dedicated DMA engine to handle complex signal processing tasks with a bus-mastering PCI interface.

The support functions ensure efficient transfer of audio data streams to and from system memory buffers, providing a system solution with maximum performance and minimal host CPU loading. The architecture enables implementation of communications over the Internet from multiple sources.

The ES1983 incorporates an HSP modem interface via its AC-Link connecting with the ES2828 MC'97 CODEC. The MC'97 is used as the analog front end for the modem and DAA control. The ES56 V.90 modem runs on the host while the ES1983 serves as the bi-directional buffer for data transmission and reception. The modem functions include the standard AT command set, V.42*bis* and Group 3 Fax.

The ES1983, which operates at 3.3 volts digitally, is compliant with the Advanced Power Management (APM) 1.2, Advanced Configuration and Power Interface (ACPI) 1.1, and PCI Power Management Interface (PPMI) 1.1. The ES1983 supports D0, D1, D2, and D3 power-saving modes for power efficiency when the audio system is both active and idle.

The ES1983 provides full DOS game compatibility through three hardware implementations: PC/PCI, Distributed DMA (DDMA), and Transparent DMA (TDMA).

The ES1983 is available in an industry-standard 100-pin Thin Quad Flat Pack (TQFP) package.

AUDIO FEATURES

- High-performance PCI audio acceleration
- Digital docking with secondary AC-Link or I^{2}S digital link
- S/PDIF digital audio input
- Multi-stream DirectSound and DirectSound 3D acceleration
- Sensaura CRL Positional 3D
- High-quality sample rate conversion and digital mixing
- AC-3 speaker virtualization
- Direct Music support
- Realtime effects processing
- S/PDIF output for DVD content
- EEPROM interface for SID and SVID
- Full legacy DOS game support using PC/PCI, DDMA, or TDMA hardware implementation methods
- Supports up to two additional PCI bus master devices
- HSP modem interface via MC'97 link

POWER MANAGEMENT

- Compliance with APM 1.2, ACPI 1.1, and PPMI 1.1
- Compliance with Intel's "Mobile Power Guidelines '99"
- 3.3 volt digital operation with 5V-tolerant inputs

COMPATIBILITY

- Supports PC games and applications for Sound Blaster^TM and Sound Blaster Pro^TM
- Supports Microsoft® Windows^TM SoundSystem^TM
- Meets PC99 and WHQL specifications
- Compliant with Intel's Audio-Modem Riser Card and mini-PCI Specifications

MODEM FEATURES

- Data Mode capabilities:
  - V.90 56K bps
  - V.34 33.6 kbps and fallbacks
  - Standard AT command set
  - V.42 (LAPM) and MNP4 error correction
  - V.42bis/MNP 5 data compression
- Fax Mode capabilities:
  - ITU-T V.17, V.21 ch2, V.27ter, V.29
  - Group 3 (TIA/EIA 578 Class 1 and Class 2)
- Supports Wakeup On Ring from **D3**$_{hot}$ and **D3**$_{cold}$ state and DAA control

CONTENTS

FIGURES

TABLES

PINOUT

Figure 1 ES1983 Maestro-3i Pinout

PIN DESCRIPTION

Name	Number	I/O	Description
C/BE[3:0]#	1, 13, 21, 31	I/O	PCI command/byte enable pins. During address phase of a transaction, these pins define the bus command. During data phase, these pins define the byte enable.
IDSE		I	ID Select.
GPIO9	2	I/O	General purpose GPIO9 I/O pin; internally pulled up to VDD.
PCGNT#		O	Use also as PC/PCI grant input pin.
GND	3, 22, 41, 63, 75, 88, 91	I	Digital ground
AD[31:0]	92:99, 4:11, 23:30, 33:40	I/O	Address and data lines from the PCI bus
VDD	12, 32, 66, 86, 100	I	Digital supply voltage, 3.3V
FRAME#	14	I/O	Cycle frame
IRDY#	15	I/O	Initiator ready
TRDY#	16	I/O	Target ready
DEVSEL#	17	I/O	Device select
STOP#	18	I/O	Stop transaction
R0#		I	Use as PCI bus request 0 input pin from external PCI master device by enabling PCIx2 arbiter bit PCI 58h [0] = 1.
GPIO2	19	I/O	General purpose GPIO2 I/O pin.
PCGNT#		O	Use also as PC/PCI grant input pin for add-in card application.
PAR	20	I/O	Parity.
I^{2}SCLK	42	I	I^{2}S serial clock input pin and is enabled by setting Maestro_Base+36h [15] to 1.
GPIO6		I/O	General purpose GPIO6 I/O pin; internally pulled up to VDD.
CLKRUN#		I/O	Used as CLKRUN#, is I/O pin for PCI Clock status and an output to start or accelerate clock function by enabling PCI 52h [11] = 1.
ECS	43	O	Chip select output pin to EEPROM chip select input. ECS goes active after power-on reset and goes inactive automatically after EEPROM cycle is complete.
I^{2}SLR	44	I	I^{2}S frame sync input pin and is enabled by setting Maestro_Base+36h [15] to 1.
GPIO12		I/O	General purpose GPIO12 I/O pin; internally pulled down to GND.
I^{2}SDATA	45	I	I^{2}S data input pin and is enabled by setting Maestro_Base+36h [15] to 1.
GPIO8		I/O	General purpose GPIO8 I/O pin; internally pulled up to VDD.
GPIO7	46	I/O	General purpose GPIO7 I/O pin; internally pulled up to VDD.
GT1#		O	Grant to PCI master directly and is enabled by PCI 58h [11] = 1 and PCI 58h [10] = 1.
GS1	47	O	Grant-Select 1 output pin to control external quick switch to grant PCI master phase and is enabled by PCI 58h [11] = 0 and PCI 58h [10] = 1.
GPIO10		I/O	General purpose GPIO10 I/O pin; internally pulled up to VDD.
R1#		I	PCI bus request 1 input pin from external PCI master device by enabling 2nd PCIx2 arbiter bit PCI 58h [10] = 1.
GPIO14	48	I/O	General purpose GPIO14 I/O pin; internally pulled up to VDD.
VOLDN#		I	Active-low signal. Hardware volume down control and is enabled by PCI 52h [7] = 1 and PCI 52h [5] = 0.
GPIO4	49	I/O	General purpose GPIO4 I/O pin; internally pulled up to VDD.
VOLUP#		I	Active-low signal. Hardware volume up control and is enabled by PCI 52h [7] = 1 and PCI 52h [5] = 0.
GPIO5	50	I/O	General purpose GPIO5 I/O pin; internally pulled up to VDD.
SDI1	51	I	Primary AC-Link serial data input; internally pulled up to VDD. Enable primary Codec by setting Maestro_Base+36h [12] = 1.
MC97DI		I	Use as Modem Codec data input pin by enabling the PCI 5Ch [5] =1 and Maestro_Base+38h [3] to 1; internally pulled up to VDD.
RING#	52	I	Ring detect pin and is enabled by PCI 5Ch [5] = 0.
PME#	53	O	PME# output pin to wake up the system by enabling PME_EN bit (C5h [0] = 1).
V$_{AUX}$	54	I	3.3V$_{AUX}$ voltage supply input pin .

Name	Number	I/O	Description
V_{AUX}Det	55	I	V_{AUX} support detection pin. V_{AUX}Det pin needs to be driven high to indicate ACPI is supported with D3$_{cold}$ state and driven low to indicate ACPI is not supported with D3$_{cold}$ state.
DI2SADC/ SDI2	56	I	Line-In from I^{2}S docking. Enable I^{2}S docking by setting Maestro_Base+38h [7] to 1.
		I	Secondary AC-link serial data input. Enable secondary Codec by setting Maestro_Base+38h [5] to 1; internally pulled up to VDD.
DI2SFS/ SDFS2	57	O	Frame sync to I^{2}S docking. Enable I^{2}S docking by setting Maestro_Base+38h [7] to 1.
		O	Secondary AC-link serial data frame sync output pin. Enable second codec by setting Maestro_Base+38h [5] to 1. If a pull-down resistor (2.2 k ohm) is used, then the device is set as a multifunction device. Otherwise, the ES1983 is set as a single-function audio-only device; internally pulled up to VDD.
DI2SDAC SDO2	58	O	Line-Out to I^{2}S docking. Enable I^{2}S docking by setting Maestro_Base+38h [7] to 1.
		O	Secondary AC-link serial data output; internally pulled down to GND. Enable second codec by setting Maestro_Base+38h [5] to 1.
DI2SCLK SCLK2	59	O	3.072 MHz clock to I^{2}S docking. Enable I^{2}S docking by setting Maestro_Base+38h [7] to 1.
		O	Secondary AC-link serial data clock output pin for multi-CODEC configurations and secondary AC-Link interface. Enable second codec by setting Maestro_Base+38h [5] to 1. Can be pulled down to GND via a 2.2 K Ohm resistor to internally fix IDSEL and leave pin 2 free for other function use.
SRST1#	60	O	Primary AC97 Codec reset output pin.
GPIO0		I/O	General purpose GPIO0 I/O pin; internally pulled up to VDD.
SRST2#		O	Secondary AC97 Codec reset output pin.
GPIO3	61	I/O	General purpose GPIO3 I/O pin; internally pulled up to VDD.
SPDIFI		I	Sony/Philips Digital Interface input. Enabled by setting Maestro_Base+3Eh [0] = 1.
SRIQ		I/O	Serialized IRQ; internally pulled up to VDD. Enabled by PCI 40h [14] = 1.
SPDIFO	62	O	Sony/Philips Digital Interface output. Enabled by PCI 52h [8] = 1 and PCI 58h [1] =0 and Maestro_Base+38h [4] = 1.
GPIO11		I/O	General purpose GPIO11 I/O pin; internally pulled up to VDD.
OSCI	64	I	49.152 MHz crystal input. Not a 5 volt tolerant pin.
OSCO	65	O	49.152 MHz crystal output.
GD[0]	67	I/O	Game port data I/O pin.
GD[1]		I/O	Game port data I/O pin.
EDOUT	68	O	Data output pin to EEPROM data input. EDOUT goes active after power-on reset goes inactive automatically after EEPROM cycle is complete.
GD[2]		I/O	Game port data I/O pin.
EDIN	69	I	Data input pin from EEPROM data output.
VOLUP#		I	Hardware volume control enabled by PCI 52h [7] = 1 and PCI 52h [5] = 1.
GD[3]		I/O	Game port data I/O pin.
ECLK	70	O	Clock output pin to EEPROM clock input. ECLK goes active after power-on reset and goes inactive automatically after EEPROM cycle is complete.
VOLDN#		I	Hardware volume down control enabled by PCI 52h [7] = 1 and PCI 52h [5] = 1.
GD[4:5]	71:72	I	Game port data input pin; internally pulled up to VDD.
DI2SMIC	73	I	Mic-In from I^{2}S docking. Enable I^{2}S docking by setting Maestro_Base+38h [7] to 1.
GD6		I	Game port data input pin; internally pulled up to VDD.
DI2SCD	74	I	CD-In from I^{2}S docking. Enable I^{2}S docking by setting Maestro_Base+38h [7] to 1.
GD7		I	Game port data input pin; internally pulled up to VDD.
SCLK1	76	I	Primary AC-Link serial clock; enabled by setting Maestro_Base+36h [12] =1. Internally pulled up to VDD.
SDFS1	77	O	Primary AC-Link serial data frame sync; enabled by setting Maestro_Base+36h [12] =1. Internally pulled up to VDD.

PIN DESCRIPTION

Name	Number	I/O	Description
SDO1	79	O	Primary AC-Link serial data out enabled by setting Maestro_Base+36h[12]=1; internally pulled up to VDD.
GT0#		O	Grant to PCI master directly by enabling PCI 58h [0] = 1 and PCI 58h [11] = 1.
GS0	78	O	Grant select 0 output pin to control external quick switch to grant PCI master phase by enabling PCIx2 arbiter bit PCI 58h [0] = 1 and PCI 58h [11] = 0.
GPIO1		I/O	General purpose GPIO1 I/O pin; internally pulled up to VDD.
TXD	80	O	MIDI transmit data output pin (default). Select as MIDI transmit output pin by enabling PCI 40h [3] = 1; internally pulled up to VDD.
RXD	81	I	MIDI receive data input pin (default). Select as MIDI receive input pin by enabling PCI 40h [3] = 1; internally pulled down to GND.
PCREQ#	82	O	Use as PC/PCI request output pin by setting PCI 50h [10:8] = 010.
GPIO13		I/O	General purpose GPIO13 I/O pin; internally pulled down to GND.
C24		O	24.576 MHz clock output fot CODEC clock source.
SPDIFO	83	O	S/PDIF output pin and is enabled by setting bit PCI 52h [8] = 1 and bit PCI 58h [1] = 1, and setting Maestro_Base+38h[4]=1.
GPIO15		O	General purpose output-only pin; internally pulled up to VDD.
RST#	84	I	Reset
INT#	85	O	Interrupt request
PCICLK	87	I	PCI bus clock
GNT#	89	I	PCI Bus master grant
REQ#	90	O	PCI Bus master request

FUNCTIONAL PIN GROUPING

Function	Pins	Pin Number
Primary (AC'97/MC'97-compatible) AC-Link Interface Pins:	SDI1 *	51
	SRST1# *	60
	SCLK1	76
	SDFS1 *	77
	SDO1 *	79
I^2S Digital Docking Interface Pins:	DI2SADC *	56
	DI2SFS *	57
	DI2SDAC*	58
	DI2SCLK *	59
	DI2SMIC *	73
	DI2SCD*	74
MC-Link Interface Pin:	MC97DI *	52
ACPI/V_{AUX} Pins	PME#*	53
	V_{AUX}	54
	V_{AUXDET} *	55
Audio Interface Pins	SPDIFO *	62, 83
	VOLUP# *	50, 69
	VOLDN# *	49, 70
	RxD *	81
	TxD *	80
Clock and Generation Pins	OSCI	64
	OSCO	65
	C24 *	83
EEPROM Interface Pins	ECS *	43
	EDOUT *	68
	EDIN *	69
	ECLK *	70
Game Port Interface Pins	GD[7:0] *	74:67

Function	Pins	Pin Number
General-Purpose I/O Pins	GPIO0 *	60
	GPIO1 *	78
	GPIO2 *	19
	GPIO3 *	61
	GPIO4 *	49
	GPIO5 *	50
	GPIO6 *	42
	GPIO7 *	46
	GPIO8 *	45
	GPIO9 *	2
	GPIO10 *	47
	GPIO11 *	62
	GPIO12 *	44
	GPIO13 *	82
	GPIO14 *	48
	GPIO15 *	83
I^{2}S Interface	I^{2}SCLK *	42
	I^{2}SLR *	44
	I^{2}SDATA *	45
PCI Bus Interface Pins and Multiple PCI Master Pins	R0# *	19
	GS0, GT0# *	78
	PCGNT# *	2
	AD[31:0]	92:99, 4:11, 23:30, 33:40
	CBE[3:0]#	1, 13, 21, 31
	FRAME#	14
	IRDY#	15
	TRDY#	16
	DEVSEL#	17
	STOP#	18
	PAR	20
	CLKRUN# *	43
	GS1, GT1# *	47
	R1# *	48
	SIRQ# *	62
	PCREQ# *	82
	RST#	84
	INT#	85
	PCICLK	87

Function	Pins	Pin Number
	GNT#	89
	REQ#	90
Power and Ground Pins	VDD	12, 32, 66, 86, 100
	GND	3, 22, 41, 63, 75, 88, 91

 * These pins share more than one function.

STRAP PINS

Pin 57	Pin 77	Pin 59	Design Platform Mode
1	1	0	Audio-only design for notebook/motherboard platform.
0	1	0	Audio-Modem combo design for notebook/motherboard platform.
1	0	1	Audio-only design for add-in card platform.
0	0	1	Audio-Modem combo design for add-in card platform.

BLOCK DIAGRAMS
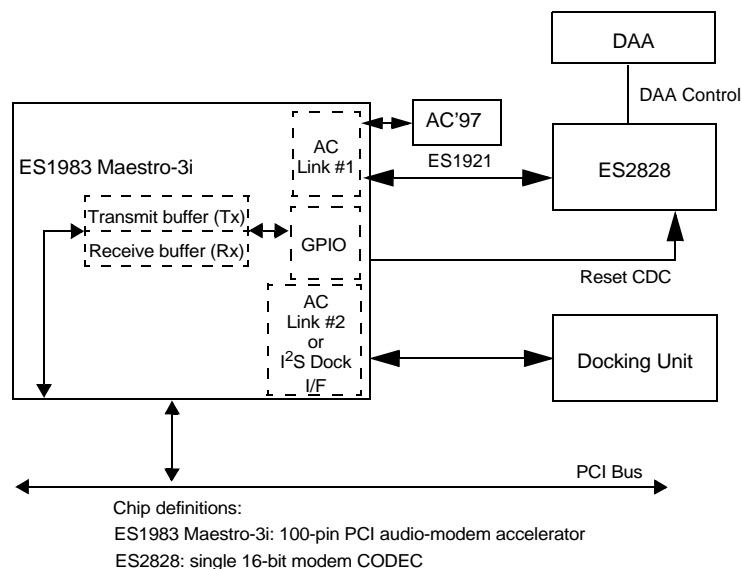
Figure 2 ES1983 System Block Diagram
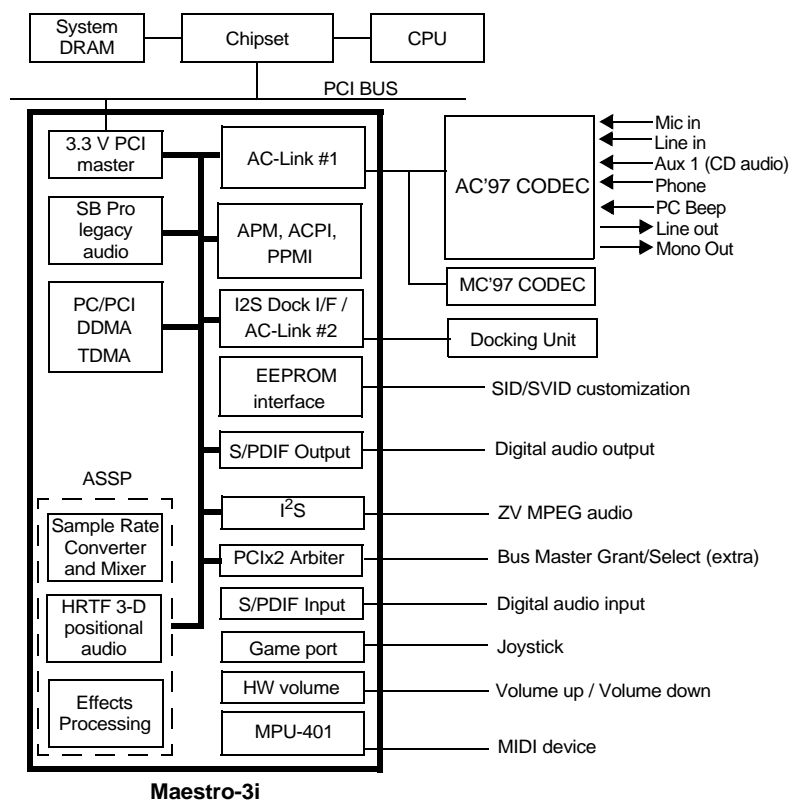
Figure 3 ES1983 Device Block Diagram

FUNCTIONAL DESCRIPTION

The ES1983 Maestro-3i PCI audio accelerator, when combined with an AC'97 and a modem AFE, forms a complete HSP-based audio-modem solution. The ES1983 provides a flexible audio-modem I/O interface to both a modem subsystem and an audio subsystem while serving as a bi-directional buffer for data transmission and reception. The ES1983 incorporates one AC'97 Extension 2.1 compliant link to interface with an external AC'97 Codec and an MC'97 compliant modem AFE and incorporates one I^{2}S I/O link to interface to a digital docking unit.

The ES1983 includes the following subsystems:

Audio Subsystems

- **AC'97 Link for Audio Codec** – provides interface to an external primary Codec and an MC'97 compliant Codec.

- **I2S Link / Secondary AC'97 Link** – provides I^{2}S interface to a docking unit or to an external secondary Codec.

- **ASSP** – FM emulation, sample rate conversion, digital mixing, 3D audio and special effects are performed by the embedded application specific signal processor.

- **PCI Bus Master** – Supports two additional PCI bus masters.

- **Dual game port** – integrated dual game port for two joysticks.

- **EEPROM Interface** – serial port connection from an EEPROM for Subsystem ID and Subsystem Vendor ID.

- **FIFO** – RAM for a 128-word FIFO data buffer as memory-mapped I/O for I/O processing.

- **Hardware volume control** – 2 pushbutton inputs with internal pull-up devices for up/down/mute that can be used to adjust the master volume control.
  The mute input is defined as the state when both up and down inputs are pressed simultaneously.

- **I^{2}S Zoom Video serial port** – supports sample rates up to 48 kHz for MPEG audio.

- **MPU-401 serial port** – asynchronous serial port for MIDI devices such as a music keyboard input.

- **Oscillator** – circuitry to support an external crystal.

- **PCI bus interface** – provides interface to 3.3/5 volt PCI bus signals. The PCI 2.2 compliant interface supports bus master/slave.

PCI Interface

The ES1983 audio accelerator features a number of dedicated registers for handling of audio data and for handling modem data during an online session and for power management. These registers include dual PCI configuration registers and power management registers.

The setting of bit 7 of the Header Type register at index 0Eh determines how the PCI configuration space of the ES1983 shall be used. When bit 7 is a 0, the ES1983 is a single-function, audio-only device. When bit 7 is a 1, however, the ES1983 becomes a multi-function audio-modem device for combo configurations. When configured as a multi-function device, the audio and modem sections will have their own PCI configuration registers. Table 1 lists the dual sets of registers.

Table 1   Dual Registers in the ES1983 Architecture

Dual Register Name	Register Index
PCI Configuration Register	
ES1983 I/O Space Base Address	10h,11h (R/W)
Interrupt Line	3Ch (R/W)
Power Management	
Next-Item Pointer	C1h (R)
Power Management Capabilities	C2h, C3h (R)
Power Management Control/Status	C4h (R/W)
PME Control	C5h (R/W)

Memory Architecture

The ES1983 includes 3K x 16 words of on-chip program RAM and 3K x 16 words of on-chip data RAM in its Application Specific Signal Processor (ASSP) module, which serves as the device's program and data memory. Additionally, the ES1983 contains a 128-word RAM as memory-mapped I/O buffer for I/O processing.

Figure 1 details the Maestro memory architecture.
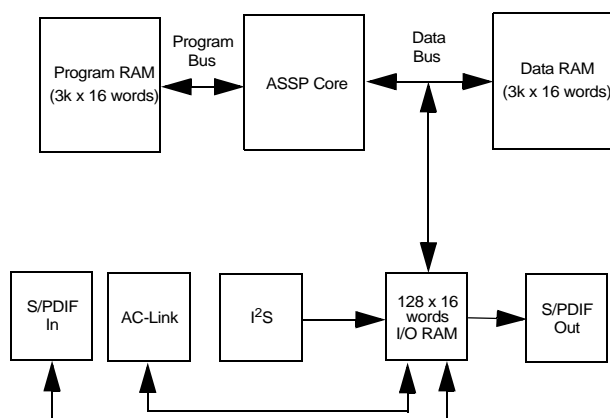
ASSP Memory Mapping

The ES1983 uses the following data and program memory maps:

- Program Memory

   0h - BFFh (3K SRAM)

- Data Memory

   500h - 5FFh (I/O SRAM)

   1000h - 1 BFFh (3K SRAM)

   2000h - 2BFFh (3K logical SRAM for FM)

ASSP I/O RAM

In the ES1983, the 128 x 16 I/O RAM is implemented by ping-pong buffer to reduce interrupt latency. The ASSP can read from I/O port 8014h to determine which bank is available. Bit 3 means the 48K Even bank status, while Bit 7 means I^{2}S Even bank status. If the relative bit is 1, the Even bank is available. If the relative bit is 0, the Odd bank is available. The ASSP can read data in from either the I^{2}S or AC-Link at the addresses listed in Table 2.

Table 2   Memory Address (Input)

Even Bank	Odd Bank	Signal Name
0500 ~ 0503	0540 ~ 0543	ADC_L
0504 ~ 0507	0544 ~ 0547	ADC_R
0508 ~ 050b	0548 ~ 054b	AC-Link dock ADC_L / I^{2}S dock ADC_L
050c ~ 050f	054c ~ 054f	AC-Link dock ADC_R I^{2}S dock ADC_R
0510 ~ 0513	0550 ~ 0553	I^{2}S_L
0514 ~ 0517	0554 ~ 0557	I^{2}S_R
0518 ~ 051b	0558 ~ 055b	I^{2}S dock CD_L/ S/PDIF_In_L
051c ~ 051f	055c ~ 055f	I^{2}S dock CD_R/ S/PDIF_In_R

The ASSP can write data out to either the AC-Link or S/PDIF at the addresses listed in Table 3.

Table 3   Memory Address (Output)

Even Bank	Odd Bank	Signal Name
0520 ~ 0523	0560 ~ 0563	DAC_L (slot 3)/ docking DAC_L
0524 ~ 0527	0564 ~ 0567	DAC_R (slot 4)/ docking DAC_R
0528 ~ 052b	0568 ~ 056b	Center (slot 6)
052c ~ 052f	056c ~ 056f	L_SUR (slot 7)
0530 ~ 0533	0570 ~ 0573	R_SUR (slot 8)
0534 ~ 0537	0574 ~ 0577	LFE_SUR (slot 9)
0538 ~ 053b	0578 ~ 057b	S/PDIF_Out_L
053c ~ 053f	057c ~ 057f	S/PDIF_Out_R

S/PDIF Interface

The S/PDIF output of the ES1983 transfers audio data in a digital format linked to the data's sampling rate. Each left or right channel of digital data is transferred in a 32-bit subframe, with two subframes making up one frame of data transferred at the 48 kHz sample rate.

The S/PDIF input of the ES1983 receives audio data only in PCM digital format linked to the data's sampling rate. Each left or right channel of digital data is recieved in a 32-bit subframe, with two subframes making up one frame of data. The S/PDIF input data can be at 32 kHz, 44.1 kHz, and 48 kHz sample rate. Each channel's subframe consists of a single digital sample up to 20 bits wide in conjunction with 12 bits of control data. 192 frames of data make up a single data block.

The S/PDIF output works in conjuction with several control/status registers located in the I/O space of the ASSP core. These registers control the functionality of the interface as well as transfer the digital audio data located in the S/PDIF data stream to and from the ASSP.

AC-Link Interface

The AC-Links of the ES1983 are bi-directional, fixed rate serial PCM digital stream interfaces that handle both multiple input and output data streams and control register accesses using a time division multiplexed scheme.

Codec Data Output Framing

The ES1983 AC-Link architecture supports up to seven outgoing data streams. Slots 0, 1, 2, 3, and 4 as defined by the AC'97 Rev. 2.1 spec are supported and comprise the ES1983 SDATA_OUT bi-directional data frame in an audio-only design. In an audio-modem design, Slots 5 and 12 are also supported for modem data framing operations.

Figure 4 shows the output and input frames supported by the integrated AC'97 Codec.
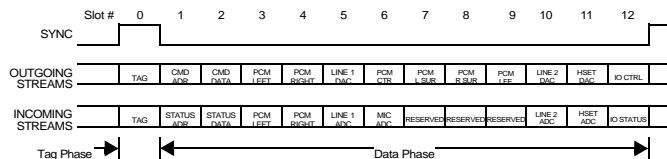
Figure 4 The ES1983 Bi-directional Data Frame

Slot 0: Tag

Within Slot 0, the first bit is a global bit that flags the validity for the entire data frame. If the valid frame bit is a 1, the current data frame contains at least one slot time of valid data. The next five bit positions sampled indicate which of the corresponding five time slots contain valid data.

Slot 1: Command Address Port

The command address port controls features and monitors status of AC'97 functions. The command address port bit assignments are listed in Table 4.

Table 4   Slot 1 Command Address Bits and Functions

Bit	Function	Description
19	Read/Write command	1 = read; 0 = write
18:12	Control Register Index	64 16-bit locations, addressed on even byte boundaries.
11:0	Reserved	Stuffed with zeroes.

Slot 2: Command Data Port

The command data port delivers 16-bit control register write data in the event the current command port operation is a write cycle. If the current command port operation is a read cycle, the entire time slot must be stuffed with zeros by the digital controller. The command data port bit assignments are listed in Table 5.

Table 5   Slot 2 Command Data Bits and Functions

Bit	Function	Description
19:4	Control Register Write Data	Stuffed with zeroes if current operation is a read.
3:0	Reserved	Stuffed with zeroes.

Slot 3, PCM Playback Left Channel and Slot 4, PCM Playback Right Channel

Audio output frame slot 3 is the composite digital audio left playback stream. Audio output frame slot 4 is the composite digital audio right playback stream. In a typical "games compatible" PC, these slots are composed of standard PCM (*.wav) output samples digitally mixed with music synthesis output samples.

Slot 5: Modem Line 1 DAC

The modem line 1 DAC resolution is by default 16 bits. During normal runtime operation, the digital controller stuffs non-valid trailing bit positions within this time slot with zeros. Slot 5 also contains the MSB justified modem DAC input data.

Slot 12: Modem General Purpose I/O Control

Up to 16 bits of modem GPIO status (input) and control (output) have been directly assigned to bits on Slot 12 in order to minimize latency of access to changing conditions.

Codec Data Input Framing

The ES1983 AC-Link architecture supports up to seven incoming data streams. Slots 0, 1, 2, 3 and 4 as defined by the AC'97 Rev. 2.1 spec are supported and comprise the ES1983 SDATA_IN bi-directional data frame in an audio-only design. In an audio-modem design, Slots 5 and 12 are also supported for modem data framing operations.

Slot 0: Tag

Within Slot 0, the first bit is a global bit that flags whether the integrated AC'97 Codec is in the Codec Ready state or not. If the Codec Ready bit is a 0, the integrated AC'97 Codec is not ready for normal operation. This condition is normal following the deassertion of power on reset, for example, while the Maestro's voltage references settle.

When the Codec Ready bit is a 1, the Control and Status Registers and the AC-Link are fully operational. The ES1983 must then further probe the Powerdown Control/Status register to determine if any further subsections, if any, are ready.

Before putting the integrated AC'97 Codec into operation, the ES1983 polls the first bit in the data input frame to ensure the integrated Codec registers have gone Codec Ready.

Once the integrated Codec registers are Codec Ready, the next five bit positions sampled by the ES1983 indicate which of the corresponding slots are assigned to input data streams, and that they contain valid data.

A new data frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the integrated Codec samples the assertion of SYNC.

This falling edge marks the time when both sides of AC-Link are aware of the start of a new data frame. On the next rising of BIT_CLK, the integrated Codec transitions SDATA_IN into the first bit position of Slot 0 (Codec Ready bit). Each new bit position is presented to AC-Link on a rising edge of BIT_CLK.

Slot 1: Status Address Port

The status address port controls features and monitors status of AC'97 functions. The status address port bit assignments are listed in Table 6.

Table 6   Status Address Port Bit Assignments

Bit	Function	Description
19	Reserved	Stuffed with zeroes.
18:12	Control Register Index	Echo of register index for which data is being returned.
11:2	SLOTREQ bits	Refer to Appendix A of the AC'97 Component Spec.
1:0	Reserved	Stuffed with zeroes.

Slot 2: Status Data Port

The status data port delivers 16-bit control register read data. If Slot 2 is tagged invalid, the slot is stuffed with zeros by the digital controller. The status data port bit assignments are listed in Table 7.

Table 7   Status Port Data Bit Assignments

Bit	Function	Description
19:4	Control Register Read Data	Stuffed with zeroes if tagged invalid.
3:0	Reserved	Stuffed with zeroes.

Slot 3, PCM Record Left Channel and Slot 4, PCM Record Right Channel

Audio input frame slot 3 is the left channel output of AC'97's input mux, post-ADC. Audio input frame slot 4 is the right channel output of AC'97's input mux, post-ADC. AC'97 ships out its ADC output MSB first.

Slot 5: Modem Line 1 ADC

The modem line 1 ADC resolution is by default 16 bits. During normal runtime operation, the digital controller stuffs non-valid trailing bit positions within this time slot with zeros. Slot 5 also contains the MSB justified modem ADC input data.

Slot 12: Modem General Purpose I/O Status

Up to 16 bits of modem GPIO status (input) and control (output) have been directly assigned to bits on Slot 12 in order to minimize latency of access to changing conditions.

Hardware and Master Volume Control

Two external pins, VOLUP# and VOLDN#, can be connected to external momentary switches to ground to implement hardware master volume controls. Pressing one of these buttons produces a low signal to one of the inputs and thereby changes the master volume. MUTE is emulated by the state where both VOLUP# and VOLDN# inputs are low simultaneously. The up and down buttons produce a single step change in volume when they are first pressed and held down. Hold each input low or high for it to be recognized as a valid button press. A software option allows the debounce time to be reduced. The two inputs have debounce circuitry within the ES1983. Setting bit 7 in the Maestro Configuration B register at index 52h/53h enables hardware volume control.

Peripheral Interfacing

I^{2}S Serial Interface

The I^{2}S input pins I^{2}SDATA, I^{2}SCLK, and I^{2}SLR are used for a serial interface to an external device and are multiplexed with other functions.

Refer to Table 9 for a description of the I^{2}S interface pins. Set bit 15 of the Maestro_Base+36h register to 1 to enable the I^{2}S input pins. A typical application of the I^{2}S serial interface is MPEG audio. See Figure 6.
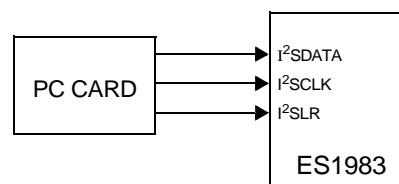
Figure 5 I^{2}S Implementation in ES1983

.

Table 8   I^{2}S Interface Pins

Pin	Description
I^{2}SDATA	Serial data for I^{2}S interface. This pin has an internal pull-up
I^{2}SCLK	Serial shift clock for I^{2}S interface.
I^{2}SLR	Left/Right signal for I^{2}S interface. This pin has an internal pull-down.

I^{2}S Serial Docking Interface

The I^{2}S docking pins DI^{2}SADC, DI^{2}SCLK, DI^{2}SCD, DI^{2}SDAC, DI^{2}SFS, and DI^{2}SMIC comprise the serial docking interface for ES1983 to an external device and are multiplexed with other functions. Refer to Table 9 for a complete description of the I^{2}S interface pins. Set bit 15 of the Maestro_Base+38h register to 1 to enable the I^{2}S docking pins.
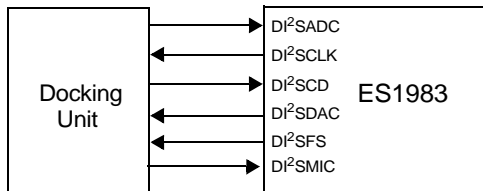
Figure 6 I^{2}S Docking Interface Implementation in ES1983

.

Table 9   I^{2}S Serial Docking Interface Pins

Pin	Description
DI^{2}SADC	Line-In serial data input from I^{2}S docking unit.
DI^{2}SCLK	3.072 MHz serial shift output clock to I^{2}S docking unit.
DI^{2}SCD	CD-In serial data input from I^{2}S docking unit.
DI^{2}SDAC	Line-Out serial data output to I^{2}S docking unit.
DI^{2}SFS	48 kHz sample frame sync output to I^{2}S docking unit.
DI^{2}SMIC	Mic-In serial data input from I^{2}S docking unit.

Joystick / MPU-401 Interface

Joystick / MIDI External Interface

The joystick portion of the ES1983 reference design is identical to that on a standard PC game control adaptor or game port. The PC compatible joystick can be connected to a 15-pin D-sub connector. It supports all standard PC joystick-compatible software. If the system already has a game card or port, remove the game card.

MPU-401 UART Mode

There is one MIDI interface (RxD and TxD) in the ES1983, an MPU-401 "UART mode" compatible serial port.

DOS Game Compatibility

ISA DMA

To emulate ISA DMA on the PCI bus, the ES1983 can employ three different protocols:

TDMA	Transparent DMA, a chipset independent mechanism
DDMA	Distributed DMA, must be supported by the PCI chipset
PC/PCI DMA	PC to PCI DMA, must be supported by the PCI chipset

Once one of the three DMA protocols is set up, the ES1983 is seen as an ISA device.

TDMA

In TDMA, the ES1983 snoops PCI bus transactions to a legacy DMA controller device then performs a PCI bus master transaction to complete DMA.

DDMA

In DDMA, the central resource (PCI chipset) includes a DMA remap engine. All transactions to legacy DMACs are remapped to each client (such as the ES1983) by the remap engine. The ES1983 then performs a PCI bus master transaction.

PC/PCI DMA

In PC/PCI DMA, the central resource (PCI chipset) performs PC/PCI cycles, which use sideband signals to the standard PCI bus. The ES1983 then acts as a slave device during DMA.

ISA IRQ

The ISA IRQ is edge triggered while PCI IRQ is level sensitive. By configuring the IRQ policy bits in PCI Configuration register 50h and IRQ select in PCI configuration register 40h, the ES1983 can emulate ISA IRQ. Setting bit 15 of Legacy Audio Control register (index 40h) to 0 allows the ES1983 to decode legacy audio addresses.

Selecting DMA/IRQ Policy

Because PCI chipsets do not all support the same DMA protocols, DMA policy should be selected according to the chipset in use. To find out which DMA policy to use, contact your ESS FAE. DMA policy is configured in PCI Configuration register 50h, bits [10:8].

HSP Modem Operation

The Maestro-3i is configureable to function as an HSP modem device, precluding the need for an external DSP or modem data pump in the modem subsystem design.

In host modem operation, the Maestro-3i has two basic functions related to modem operation:

1. Bidirectional circular buffer:

   • Received data is sampled by the modem Codec at various frequencies: 7.2, 8.0, 9.0, 9.6, 10.287, and 16 kHz depending on the sample rate. The sample rate (16 bits per sample) is put into the receive buffer before being sent to the host.

   • Transmitted data from the host (PCI bus) is put into the transmit buffer in synchronization with the receive buffer.

   • Every six samples (configurable), the Maestro-3i checks the buffer and generates an interrupt to the host if the buffer has 12 (configurable) or more samples and lets the host perform I/O read/write. The interrupt is level sensitive.

2. DAA control

   • To make a modem functional, the following control lines are recommended: (US/NA version only; no handset; universal DAA support)

      OH   Off hook

      RI   Ring indicator

      CID   Caller ID (for voice applications)

      DAA_PM   DAA power control

      Reset_CDC Reset modem Codec

   • Full DAA interface

D3$_{cold}$ Wake-Up On Ring

Figure 7 graphically describes the basic D3$_{cold}$ wake-up on ring operation with the ES1983 and ES2828 involved.
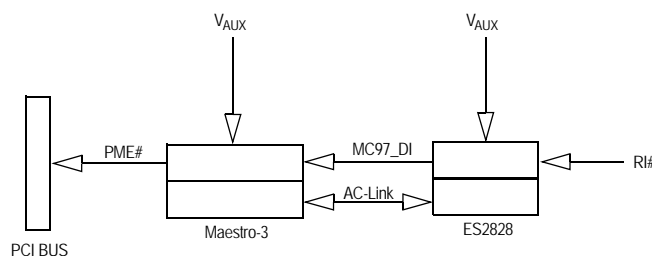
Figure 7   D3$_{cold}$ Wake-Up On Ring Sequence

D3$_{cold}$ wake-up on ring operation applies only to a combo Audio-Modem design, with split partition, where a separate audio Codec and modem Codec are used. When the system enters D3$_{cold}$ state, most of the circuit powered by D$_{VDD}$ and A$_{VDD}$ are turned off completely, with the exception of a small partition that is kept running via the V$_{AUX}$ power.

V$_{AUX}$ provides minimal power to the ES1983 and the ES2828 so that the Ring event can be detected and the complete system can be awakened by asserting the PME# signal to the system core logic. When a Ring event occurs on RI#, the MC97_DI of the ES2828 changes from low to high. The rising edge of MC97_DI causes the ES1983 digital controller to assert its PME# to the system's ACPI controller. The PME# assertion in turn causes the system to restore the DVDD and AVDD power and service the modem event initiated by the Ring event.

Once system power is restored, the device drivers execute either a cold or warm reset to the AC-Link interfaces and restore all register contents that were saved prior to entering the D3$_{cold}$ state. The MC97_DI signal from the ES2828 remains high until a cold or warm reset to the AC-Link is executed.

Ring In Enable

When the ES1983 is paired with a modem Codec, setting bit 0 of the Maestro Configuration B register at index 52h/53h enables the RING_IN function to be received at GPIO0 of slot 12 in MC'97 AC-Link.

Data and Fax Modes

In audio-modem configuration, the ES1983 supports all data modem standards up to 56 Kb/s. Modulations and data rates conform to the following standards:

   • ITU V.90

   • ITU V.34

   • ITU V.32*bis*

   • ITU V.32

   • ITU V.22*bis*

   • ITU V.22

   • ITU V.21

   • Bell 212A

   • Bell 103

V.42/MNP 2-4 error correction and V.42*bis*/MNP 5 data correction reduce error transmission and improve data throughput. The default AT command set is TIES (Time Independent Escape Sequence). The Hayes escape sequence, which is time dependent, is optionally supported. Both escape sequences are universally accepted by communications software programs. The Fax AT command set is compatible with EIA/TIA-578 Class 1 and Class 2 standards. Fax transmit and receive speeds up to 14.4 Kb/s are available. Fax modulations and data rates conform to the standards appearing in Table 10 and Table 11

.

Table 10 Fax Modes Supported

ITU Mode	Data Rate (kb/s)	Modulation
V.17	14.4	TCM
	12.0	TCM
	9.6	TCM
	7.2	TCM
V.21ch2	0.3	FSK
V.27ter	4.8	DPSK
	2.4	DPSK
V.29	9.6	QAM
	7.2	QAM
	4.8	QAM

Table 11 Data Modes Supported

ITU Mode	Data Rate (kb/s)	Modulation
V.90	56	PCM
V.34	33.6	TCM
	31.2	TCM
	28.8	TCM
	26.4	TCM
	24.0	TCM
	21.6	TCM
	19.2	TCM
	16.8	TCM
	14.4	TCM
	12.0	TCM
	9.6	TCM
	7.2	TCM
	4.8	TCM
	2.4	TCM
V.32*bis*	14.4	TCM
	12.0	TCM
	9.6	TCM
	7.2	TCM
	4.8	TCM
V.32	9.6	TCM
	9.6	QAM
	4.8	QAM
V.22*bis*	2.4	QAM
V.22	1.2	DPSK
V.21	0.3	FSK
Bell 212A	1.2	DPSK
Bell 103	0.3	FSK

Support for Modem Wakeup

Support for PME# event generation, modem wakeup, ring input status, time stamp for ring and DAA data I/O is provided by the ES1983 at the register level.

- Modem Wakeup Control (Maestro_Base+40h/41h): This register enables PME# event generation from ring input when PME#_RI bit 4 (Maestro_Base+40h) is enabled.

- DAA Data I/O Port (Maestro_Base+50h/+51h): This register handles ring data input from the external secondary AC'97 Codec. PCI 52h [0] needs to be enabled to support this function.

- Ring input status bit 2 (Maestro_ Base+42h/43h)

- Time stamp 0 and 1 for ring (Maestro_Base+4Ah/4Bh and Maestro_Base+4C/4Dh).

PCI Configuration Registers

Vendor ID   (00h, 01h, R)

Vendor ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	Vendor ID	Identifies ESS as the manufacturer of this device. The ID for ESS is 125Dh.

Device ID (Audio: Function 0)   (02h, 03h, R)

Device ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	Device ID	Identifies the ES1983 Maestro-3i. The ID 1998h is for audio function (function 0) and is assigned by ESS Technology, Inc.

Device ID (Modem: Function 1)   (02h, 03h, R)

Device ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	Device ID	Identifies the ES1983 Maestro-3i. The ID is 1999h for modem function (function 1) and is assigned by ESS Technology, Inc.

Command (Audio: Function 0)   (04h, 05h, R/W)

0													BM	MS	IO
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:3	–	Read-only. Returns 0 when read.
2	BM	Bus Master enable/disable. 1 = Enable bus master. 0 = Not bus master.
1	MS	Memory Space access enable/disable. 1 = Enable. 0 = Disable.
0	IO	I/O Space access enable/disable. 1 = Enable I/O space access. 0 = Disable I/O space access.

Command (Modem: Function 1)   (04h, 05h, R/W)

0													0	0	IO
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:3	–	Read-only. Returns 0 when read.
2	–	Read-only. Set to 0.
1	–	Read-only. Set to 0.
0	IO	I/O Space access enable/disable. 1 = Enable I/O space access. 0 = Disable I/O space access.

Status   (06h, 07h, R)

Status															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	–	Read-only. Returns 0290h when read.

Revision ID   (08h, R)

Revision ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	Revision ID	Identifies the revision of this device. The ID 10h is assigned by ESS Technology, Inc.

Programming Interface Identifier   (09h, R)

Programming interface identifier							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	PII	Identifies the programming interface of this device. The ID 00h indicates a default interface.

Sub-Class Code (Function 0)   (0Ah, R)

Sub-Class code							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	SCC	Identifies the type of sub-class of this device. The ID 00h indicates an audio device.

Sub-Class Code (Function 1)   **(0Ah, R)**

Sub-Class code							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	SCC	Identifies the type of sub-class of this device. The ID 80h indicates a modem device.

Base Class Code (Audio: Function 0)   **(0Bh, R)**

Base class code							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	BCC	Identifies the type of base class of this device. The ID 04h indicates a multimedia device (function 0).

Base Class Code (Modem: Function 1)   **(0Bh, R)**

Base class code							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	BCC	Identifies the type of base class of this device. The ID 07h indicates a simple communication device.

Cache Line Size   **(0Ch, R/W)**

Cache line size							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	CLS	Identifies the cache line size of this device as 00h.

Latency Timer   **(0Dh, R/W)**

Latency timer					0		
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:3	LT	Number of clocks times 8 (read-write for audio. Returns 0 when read for modem).
2:0	–	Read-only. Returns 0s when read.

Header Type   **(0Eh, R)**

SM	Configuration space layout						
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	SM	Single-/multi-function device. The ES1983 supports both audio-only single-function and multi-function audio-modem device operations. 1 = Multi-function device when used in an audio-modem configuration. 0 = Single-function device when used in an audio-only configuration.
6:0	CSL	Configuration space layout. Read-only. Defines layout for bytes 10h and up of the PCI configuration space header. ES1983 supports a 00h header type.

BIST Capability   **(0Fh, R)**

Built-in self test capability							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	BIST	Built-in self test capability is 00h.

**I/O Space Base Address
(Audio: Function 0)**   **(10h, 11h, R/W)**

IOSB[15:8]								0							ISI
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:8	IOSB[15:8]	I/O space base address. 256-bytes I/O space.
7:1	–	Reserved. Always write 0.
0	ISI	I/O space indicator. Hardwired to 1.

**I/O Space Base Address
(Modem: Function 1)**   **(10h, 11h, R/W)**

IOSB[15:8]								0							ISI
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:8	IOSB[15:8]	I/O space base address. 256-byte.
7:1	–	Reserved. Always write 0.
0	ISI	I/O space indicator. Hardwired to 1.

Memory Space Base Address
(Audio: Function 0) (14h – 17h, R/W)

MEMSB															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

MEMSB		Reserved									PF	TYPE		MSI
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
31:13	MEMSB	Memory space base address. 8192-byte.
12:4	–	Reserved. Always write 0.
3	PF	Always 0. Not prefetchable.
2:1	TYPE	Always 00. Indicates address can be located anywhere in 32-bits address space.
0	MSI	Memory space indicator. Hardwired to 0.

Subsystem Vendor ID (2Ch, 2Dh, R/W)

Subsystem Vendor ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	SVID	Read/write protected. If EEPROM is present, the power-on default is read from EEPROM; otherwise, the default value is 125Dh. There are two ways to customize the SVID: (1) set the PCI 50h[0] to 1 and write the new SVID to registers 2Ch and 2Dh, or (2) write the new SVID directly to the shadow registers 6Ch and 6Dh.

Subsystem ID (2Eh, 2Fh, R/W)

Subsystem ID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	SID	Read/write protected. If EEPROM is present, the power-on default is read from EEPROM; otherwise, the default value is 1998h. There are two ways to customize the SID: (1) set the PCI 50h[0] to 1 and write the new SID to registers 2Eh and 2Fh, or (2) write the new SID directly to the shadow registers 6Eh and 6Fh.

Capability Pointer (34h, R)

Capability pointer							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	CP	This register provides a pointer into the PCI configuration header where the PCI power management register block resides. PCI header doublewords at C0h and C4h contain the power management registers. This register is read-only and returns C0h when read.

Interrupt Line
(Audio: Function 0) (3Ch, R/W)

Interrupt line							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	IL	Interrupt line routing information. Indicates which system interrupt pin the ES1983 is connected to. The POST software writes the routing information to the Interrupt Line register as the system is initialized and configured. The value in this register depends on the system architecture. In x86-based PC systems, the values of 0 to 15 correspond with IRQ numbers 0 through 15, and the values from 16 to 254 are reserved. The value of 255 (Maestro-3's default power-up value) signifies either "unknown" or "no connection" for the system interrupt. The default value is FFh. Bits [4:0] are read/write. Bits [7:5] = bit [4].

Interrupt Line
(Modem: Function 1) (3Ch, R/W)

Interrupt line							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	IL	Interrupt line routing information. Indicates which system interrupt pin the ES1983 is connected to. The POST software writes the routing information to the Interrupt Line register as the system is initialized and configured. The value in this register depends on the system architecture. In x86-based PC systems, the values of 0 to 15 correspond with IRQ numbers 0 through 15, and the values from 16 to 254 are reserved. The value of 255 (ES1983's default power-up value) signifies either "unknown" or "no connection" for the system interrupt. The default value is FFh. Bits [4:0] are read/write. Bits [7:5] = bit [4].

Interrupt Pin   **(3Dh, R)**

Interrupt pin							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	IP	Interrupt pin information. Indicates which interrupt pin the ES1983 is using. This register is read-only and returns 01h when read, which indicates INTA#.

Minimum Grant   **(3Eh, R)**

Minimum grant							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	MG	Min_Gnt. Identifies the burst period needed. This register is read-only and returns 02h when read, which corresponds to 500 ns, and returns 00h for modem.

Maximum Latency   **(3Fh, R)**

Maximum latency							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	ML	Max_Lat. Identifies how often bus access is needed. This register is read-only and returns 18h when read, which corresponds to 6 ms, and returns 00h for modem.

Legacy-Compatible Audio Registers

Legacy Audio Control   **(40h, 41h, R/W)**

LA	SIR	MIDIIRQ			SBIRQ			DMACH		IA	MQ	MI	GM	FM	SB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15	LA	Legacy audio disable. 1 = Disable legacy audio (default). 0 = Enable legacy audio.
14	SIR	Serial IRQs enable. 1 = Enable serial IRQs. 0 = Disable serial IRQs (default).

Bits	Name	Description
13:11	MIDIIRQ	MIDI I/O IRQ select. Read-only. Default to 010.

10:8   SBIRQ   Sound Blaster IRQ select.

Bit 10	Bit 9	Bit 8	IRQ Selection
0	0	0	IRQ5 (default)
0	0	1	IRQ7
0	1	0	IRQ9
0	1	1	IRQ10
1	x	x	Reserved

7:6   DMACH   Sound Blaster DMA channel select.

Bit 7	Bit 6	DMA Channel Selection
0	0	Channel 0
0	1	Channel 1 (default)
1	0	Reserved
1	1	Channel 3

Bits	Name	Description
5	IA	I/O address aliasing control. 1 = Enable address aliasing (default). Selects 10-bit I/O. 0 = Disable address aliasing.
4	MQ	MPU-401 IRQ enable. 1 = Enable MPU-401 IRQ (default). 0 = Disable MPU-401 IRQ.
3	MI	MPU-401 I/O enable. 1 = Enable MPU-401 I/O (default). 0 = Disable MPU-401 I/O.
2	GM	Game port enable. 1 = Enable game port (default). 0 = Disable game port.
1	FM	FM synthesis enable. 1 = Enable FM synthesis (default). 0 = Disable FM synthesis.
0	SB	Sound Blaster enable. 1 = Enable Sound Blaster channel (default). 0 = Disable Sound Blaster channel.

Legacy Audio Support

The ES1983 supports the following legacy audio addresses.

Table 12 Supported Legacy Audio Addresses

Legacy Audio Resources	I/O Address Base
Sound Blaster Pro	220h/240h
FM synthesis	388h/389h/38Ah/38Bh
MPU-401	300h/320h/330h/340h
DMA	Channel 0, 1, 3
IRQ	5, 7, 9, 10

Maestro Configuration A   (50h, 51h, R/W)

SBI	PIC1	PIC0	GM	SG	DMAP			PW	IEM	--	M4D		S2	SD	S(V)ID
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15	SBI	Sound Blaster IRQ mask. 1 = Set this bit to enable IRQ masking when bit [10] = 1.
14	PCI1	PCI snoop mode 1. 1 = Set this bit in DOS mode when ES1983 PCI IRQ is not assigned to IRQ5/7/9/10.
13	PCI0	PCI snoop mode 0. 1 = Set this bit in DOS mode when ES1983 PCI IRQ is assigned to IRQ5/7/9/10.
12	GM	High-performance game port mode enable. 1 = Enable game port. 0 = Disable game port.
11	SG	Safeguard in TDMA mode, when bits [10:8] = 001. 1 = Set this bit to enable ISA merge during IOR 08h. ISA write-back in AutoDMA mode, when bits [10:8] = 100. 1 = Set this bit to enable ISA write-back in AutoDMA mode.

10:8 DMAP ISA DMA policy.

Bit 10	Bit 9	Bit 8	DMA Policy
0	0	0	Distributed DMA
0	0	1	Transparent DMA
0	1	0	PC/PCI DMA
0	1	1	Reserved
1	0	0	ISA write-back every 16 transfers
1	0	1	ISA write-back every 4 transfers
1	1	0	ISA write-back every 2 transfers
1	1	1	ISA write-back every transfer

Bits	Name	Description
7	PW	EN_PW. Posted write enable. 1 = Enable ES1983 posted write. 0 = Disable ES1983 posted write.
6	IEM	Emulate ISA timing on PCI. 1 = Use PCI timing. 0 = Emulate ISA timing.
5	--	Reserved.

4:3 M4D MPU_401_DECODE.

Bit 4	Bit 3	MPU-401 I/O
0	0	33x
0	1	30x
1	0	32x
1	1	34x

Bits	Name	Description
2	S2	SB240. Sound Blaster decode. 1 = Sound Blaster decode is 24x. 0 = Sound Blaster decode is 22x.

Bits	Name	Description
1	SD	Subtractive decoding. Write: 1 = Delay PCI grant by 1 clock during PCI master cycle and enable the detection of PCI subtractive decoding. Read: 1 = Subtractive decoding is detected.
0	SID	Write-enable bit for PCI subsystem ID (SID) and subsystem vendor ID (SVID). (registers 2CH-2Fh) 1 = SID and SVID are read/write. 0 = SID and SVID are read-only (default). Note: Registers 6Ch-6Fh are always writable

Maestro Configuration B   (52h, 53h, R/W)

ICx	CIS	CxS		PMC	CLKSL		SEN	HWV	DHE	HVI	ICD	MW	CxMS	--	RIE
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15	ICx	Internal clock multiplier enable. 1 = Enable internal clock multiplier. 0 = Disable internal clock multiplier.
14	CIS	ES1983 clock input select. 1 = Select the 49 MHz clock from the internal clock multiplier. 0 = Select clock from the external crystal oscillator input (OSCI).

13:12 CxS Clock multiplier mode select.

Bit 2	Bit 13	Bit 12	Mode
0	0	0	Mode 0
0	0	1	Mode 1
0	1	0	Mode 2
0	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5
1	1	0	Mode 6
1	1	1	Mode 7

Bits	Name	Description
11	PMC	Power management control for CLKRUN# enable. 1 = Enable PM control for CLKRUN#. 0 = Disable PM control for CLKRUN#.

10:9 CLKSL Clock divider select for Sound Blaster.

Bit 10	Bit 9	Clock Divider
0	0	Divided by 48
0	1	Divided by 49
1	0	Divided by 50
1	1	Reserved

Bits	Name	Description
8	S EN	S/PDIF enable. 1 = Enable S/PDIF output. 0 = Disable S/PDIF output (default).
7	HWV	Hardware volume control enable. 1 = Enable hardware volume control. 0 = Disable hardware volume control.

Bits	Name	Description
6	DHE	Reduced debounce for hardware volume control enable. 1 = Enable reduced debounce. 0 = Disable reduced debounce.
5	HVI	Up/down hardware volume button input select. 1 = Select input from pin 70 and 69. 0 = Select input from pin 49 and 50.
4	ICD	Internal Clock Direction 1 = Switch internal clock source from PCI clock to a 49.152 MHz clock source controlled by CIS (bit 14). 0 = Select 33 MHz PCI clock as the internal clock source. (Do not switch internal clock source).
3	MW	Writable EEPROM Interface Enable. 1 = Enable writable EEPROM interface. 0 = Disable writable EEPROM interface.
2	CxMS	Clock Multiplier Mode Select. Used along with CxS (bits 13:12) to support eight modes of clock multiplier.
1	--	Reserved.
0	RI_E	Ring In Enable. 1 = Enable Ring In from GPIO0 in slot 12 of modem codec. 0 = Disable Ring In.

ACPI Power Management Registers

ACPI Control A   (54h, 55h, R/W)

12	24	-	SPDIF	GLUE	—	PIF	HV	-	ASSP	SB	FM	ASC	MIDI	GP	—
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

The ACPI Control A register sets the state (D1 or D2) of the stop clock for each module.

Bit Definitions:

Bits	Name	Description
15	12	ACPI stop clock control for the 12 MHz clock to the secondary Codec output. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
14	24	ACPI stop clock control for the 24 MHz clock to the external AC97 Codec. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
13	--	Reserved.
12	SPDIF	ACPI stop clock control for SPDIF. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
11	GLUE	ACPI stop clock control for GLUE. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.

Bits	Name	Description
10	--	Reserved.
9	PIF	ACPI stop clock control for the PCI interface. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
8	HV	ACPI stop clock control for HW volume control. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
7	--	Reserved.
6	ASSP	ACPI stop clock control for the ASSP interface. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
5	SB	ACPI stop clock control for Sound Blaster. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
4	FM	ACPI stop clock control for FM. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
3	ASC	ACPI stop clock control for primary codec control. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
2	MIDI	ACPI stop clock control for MIDI. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
1	GP	ACPI stop clock control for the game port. 1 = Set stop clock to state D2. 0 = Set stop clock to state D1.
0	–	Reserved.

ACPI Control B   (56h, 57h, R/W)

12	24	-	SPDIF	GLUE	—	PIF	HV	—	ASSP	SB	FM	ASC	MIDI	GP	—
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

The ACPI Control B register enables the clock at the state (D1 or D2) set for each module in the ACPI Control A register.

Bit Definitions:

Bits	Name	Description
15	12	ACPI stop clock enable for the 12 MHz clock to the secondary Codec output. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
14	24	ACPI stop clock enable for the 24 MHz clock to the internal AC97 Codec. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
13	–	Reserved.
12	SPDIF	ACPI stop clock enable for SPDIF. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.

Bits	Name	Description
11	GLUE	ACPI stop clock enable for GLUE. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
10	–	Reserved.
9	PIF	ACPI stop clock enable for the PCI interface. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
8	HV	ACPI stop clock enable for HW volume control. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
7	–	Reserved.
6	ASSP	ACPI stop clock enable for the ASSP interface. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
5	SB	ACPI stop clock enable for Sound Blaster. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
4	FM	ACPI stop clock enable for FM. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
3	ASC	ACPI stop clock enable for primary codec control. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
2	MIDI	ACPI stop clock enable for MIDI. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
1	GP	ACPI stop clock enable for the game port. 1 = Enable stop clock at state D1/D2. 0 = Stop clock at state D1/D2 disabled.
0	–	Reserved.

User Configuration A (58h, 59h, R/W)

RLE	RE3	–	SC	QS	Px2	–	24	DSC	–	TB1	TB2	–	SO	×2
15	14	13	12	11	10	9	8	7	6	5	4	3 2	1	0

Bit Definitions:

Bits	Name	Description
15	RE	REQ# Low at D3 State Enable. 1 = Enables driving PCI REQ# low at D3 state.
14	RE3	REQ# Tri-state at D3 State Enable 1 = Enable tri-state of REQ# at D3 state.
13	–	Reserved.
12	SC	Stop Clock enable for external crystal oscillator 1 = Enable stop clock of crystal osc. at D3 state.
11	QS	Enable external PCI master support without Quick Switch 1 = Enable support.

Bits	Name	Description
10	Px2	2nd PCIx2 arbiter enable. 1 = Enable 2nd PCIx2 arbiter 0 = Disable 2nd PCIx2 arbiter
9	–	Reserved.
8	24	12 MHz clock input to clock multiplier. 1 = Select input clock from divider of external crystal oscillator clock (OSCI). 0 = Select input clock from BITCLK of AC-Link 1 (SCLK1).
7	DSC	Disable Stop Clock for C24 output at any power state. 1 = Disable. 0 = Enable.
6	–	Reserved.
5	TB1	Tri-state Buffer enable for C24 at D3hot state
4	TB2	Tri-state Buffer enable for any output buffer except for C24.
3:2	–	Reserved.
1	SO	SPDIF output select 1 = Set SPDIF output to pin 83. 0 = Set SPDIF output to pin 62 (default).
0	PCI×2	1st PCIx2 Arbiter Enable. Default = 0. 1 = Enable 1st PCI master support. 0 = Disable 1st PCI master support (default).

User Configuration B (5Ah, 5Bh, R/W)

Reserved										DA		–			1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:6	--	Reserved.
5	DA	DDMA addressing decode. 1= Disable decoding of DDMA addressing with I/O space enable bit.
4:1	–	Reserved.
0	1	Reserved. Must write 1.

User Configuration C (5Ch, 5Dh, R/W)

Reserved										RIS	PM GM	–	PMGS1	–	PMGS2
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:6	–	Reserved. Must write 0.
5	RIS	Ring input select. 1 = Select MC97-DI input from pin 52. 0 = Seclect ring input from MC97-DI.

Bits	Name	Description
4	PMGM	PME# MC97 Enable. 1 = PME# generation enabled from MC97_DI input pin.
3	–	Reserved.
2	PMGS1	PME# SDI1 Enable 1 = PME# generation enabled from SDI1 input.
1	–	Reserved.
0	PMGS2	PME# SDI2 Enable 1 = PME# generation enabled from SDI2 input.

Distributed DMA Control   60h, 61h, R/W)

DMA[15:4]												0	0	0	DE
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:4	DMA[15:4]	Distributed DMA base address.
3:1	--	Always write 0.
0	DE	Distributed DMA enable. 1 = Enable distributed DMA. 0 = Disable distributed DMA.

Subsystem Vendor ID Shadow   (6Ch, 6Dh, R/W)

Subsystem Vendor ID Shadow															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	SVID	Subsystem Vendor ID.

Subsystem ID Shadow   (6Eh, 6Fh, R/W)

Subsystem ID Shadow															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	SID	Subsystem ID.

Capability ID   (C0h, R)

Capability ID							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	CID	This register identifies the linked list item as the register for PCI power management. This register is read-only and returns 01h when read, which is the unique ID assigned by the PCI SIG for the PCI location of the capabilities pointer and the value.

Power Management Registers

Next-Item Pointer   (C1h, R)

Next-Item pointer							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NIP	This register is used to indicate the next item in the linked list of the PCI power management capabilities. Since ES1983 functions only include one capabilities item, this register is read-only and returns 00h.

Power-Management
Capabilities (Function 0)   (C2h, C3h, R)

PMES					D2S	D1S	–			DSI	–	PMEC	VER		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:11	PMES	PME_Support. This five-bit field indicates the power states in which the function may assert PME#. A value of 0 for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. Bit [15] = 0. PME# cannot be asserted from $D3_{cold}$. Bit [14] = 1. PME# can be asserted from $D3_{hot}$. Bit [13] = 1. PME# can be asserted from D2. Bit [12] = 1. PME# can be asserted from D1. Bit [11] = 0. PME# cannot be asserted from D0.
10	D2S	D2S. This bit indicates that this function supports the D2 power management state. 1 = D2 power management is supported.
9	D1S	D1S. This bit indicates that this function supports the D1 power management state. 1 = D1 power management is supported.
8:6	–	Reserved.Always 0.
5	DSI	The Device Specific Initialization bit indicates whether special initialization of this function is required before the generic class device driver is able to use it. Always 1.
4	–	Reserved.

Bits	Name	Description
3	PMEC	PME clock. This bit indicates that no PCI clock is required for the function to generate PME#. Value of bit 3 = 0.
2:0	VER	Version. This 3-bit field indicates that this function complies with Revision 1.0 of the PCI Power Management Interface specification. Always 010.

Power-Management
Capabilities (Function 1)   (C2h, C3h, R)

PMES					D2S	D1S	AUXC			DSI	–	PMEC	VER		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

The initial value of this register for Function 1 is read from the EEPROM. If EEPROM is not used, the default value will be F6A2h when V_{AUXDET} at pin 55 is open or pulled up or 9622h when V_{AUXDET} at pin 55 is pulled down.

Bit Definitions:

Bits	Name	Description
15:11	PMES	PME_Support. This five-bit field indicates the power states in which the function may assert PME#. A value of 0 for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. Bit [15] = 1. PME# can be asserted from $D3_{cold}$ when V_{AUXDET} is open or pulled up. Bit [15] = 0. PME# cannot be asserted from $D3_{cold}$ when V_{AUXDET} is pulled down. Bit [14] = 1. PME# can be asserted from $D3_{hot}$. Bit [13] = 1. PME# can be asserted from D2. Bit [12] = 1. PME# can be asserted from D1. Bit [11] = 0. PME# cannot be asserted from D0.
10	D2S	D2S. This bit indicates that this function supports the D2 power management state. 1 = D2 power management is supported.
9	D1S	D1S. This bit indicates that this function supports the D1 power management state. 1 = D1 power management is supported.
8:6	AUXC	V_{AUX} auxilliary current requirement. 010 = 100 mA (Max.) is required for modem function with V_{AUX} support in D3cold state. 000 = Modem w/o V_{AUX}. Function 1.
5	DSI	The Device Specific Initialization bit indicates whether special initialization of this function is required before the generic class device driver is able to use it. Always 1.
4	–	Reserved.
3	PMEC	PME clock. This bit indicates that no PCI clock is required for the function to generate PME#. Value of bit 3 = 0.

Bits	Name	Description
2:0	VER	Version. This 3-bit field indicates that this function complies with Revision 1.0 of the PCI Power Management Interface specification. Always 010.

Power-Management
Control/Status (Function 0)   (C4h, R/W)

0	0	0	0	0	0	PWR STATE	
7	6	5	4	3	2	1	0

The default value of this register 00h. This register determines and changes the current power state of the ES1983 function. The contents of this register are not affected by the internally-generated reset caused by the transition from the $D3_{hot}$ to D0 state.

Bit Definitions:

Bits	Name	Description
7:2	–	Bits [7:2] are read-only and return 0 when read.
1:0	PS	Power state. This 2-bit field is used both to determine the current power state of a function, and to set the function into a new power state.

Bit 1	Bit 0	Power State
0	0	D0
0	1	D1
1	0	D2
1	1	D3

Power-Management
Control/Status (Function 1)   (C4h, R/W)

0	0	0	0	0	0	PWR STATE	
7	6	5	4	3	2	1	0

The default value of this register 00h. This register determines and changes the current power state of the ES1983 function. The contents of this register are not affected by the internally-generated reset caused by the transition from the $D3_{hot}$ to D0 state.

Bit Definitions:

Bits	Name	Description
7:2	–	Bits [7:2] are read-only and return 0 when read.
1:0	PS	Power state. This 2-bit field is used both to determine the current power state of a function, and to set the function into a new power state.

Bit 1	Bit 0	Power State
0	0	D0
0	1	D1
1	0	D2
1	1	D3

PME Control (Function 0)　　　　**(C5h, R/W)**

PME ST	0	0	0	0	0	0	PME EN
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	PME ST	PME# status. Read for PME# Status regardless of PMEEN bit. 1 = PME# is active. 0 = PME# is inactive. Write 1 to clear status bit and cause function to stop asserting PME# pin (if enabled).
6:1	–	Bits [6:1] are read-only and return 0 when read.
0	PME EN	PME# enable. 1 = Enable PME. 0 = Disable PME.

PME Control (Function 1)　　　　**(C5h, R/W)**

PME ST	0	0	0	0	0	0	PME EN
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	PME ST	PME# status. Read for PME# Status regardless of PMEEN bit. 1 = PME# is active. 0 = PME# is inactive. Write 1 to clear status bit and cause function to stop asserting PME# pin (if enabled).
6:1	–	Bits [6:1] are read-only and return 0 when read.
0	PME EN	PME# enable. 1 = Enable PME. 0 = Disable PME.

Maestro I/O Registers

**Host Interrupt
Control**　　　　**(Maestro_Base+19h, R/W)**

MR	–	–	–	–	PGE	–	CRC
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	MR	ES1983 software reset enable. 1 = Enable ES1983 software reset. 0 = Disable ES1983 software reset.
6:3	–	Reserved.
2	PGE	Hardware volume control to PME# generation enable. 1 = Enable. 0 = Disable.
1	–	Reserved.
0	CRC	CLKRUN# generation clock. 1 = Toggle CLKRUN# when CLKRUN# is enabled. 0 = Do not toggle CLKRUN#.

**Host Interrupt
Control**　　　　**(Maestro_Base+18h, R/W)**

–	HIE	RIE	DIE	–		MIE	SIE
7	6	5	4	3	2	1	0

Bit Definitions

Bits	Name	Description
7	–	Reserved.
6	HIE	Hardware volume control interrupt enable. 1 = Enable hardware volume control interrupt. 0 = Disable hardware volume control interrupt.
5	RIE	Ring interrupt enable 1 = Enable ring interrupt. 0 = Disable ring interrupt.
4	DIE	ASSP software interrupt enable. 1 = Enable ASSP software interrupt. 0 = Disable ASSP software interrupt.
3:2	–	Reserved.
1	MIE	MPU-401 interrupt enable. 1 = Enable MPU-401 interrupt. 0 = Disable MPU-401 interrupt.
0	SIE	Sound Blaster interrupt enable. 1 = Enable Sound Blaster interrupt. 0 = Disable Sound Blaster interrupt.

Host Interrupt Status   **(Maestro_Base+1Ah, R/W)**

–	IHWV	RI	ID	Reserved		IM	BS
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	–	Reserved.
6	IHWV	Hardware volume control interrupt. 1 = Hardware volume control interrupt pending. 0 = No hardware volume control interrupt. Write 1 to clear pending interrupt request.
5	RI	Ring indicator interrupt. (read only) 1 = Ring interrupt pending. 0 = No ring indicator interrupt.
4	ID	ASSP software interrupt. (read only) 1 = ASSP interrupt pending. 0 = No ASSP interrupt.
3:2	--	Reserved.
1	IM	MPU-401 receive interrupt. (read only) 1 = MPU-401 receive interrupt pending. 0 = No MPU-401 receive interrupt.
0	BS	Sound Blaster interrupt. (read only) 1 = Sound Blaster interrupt pending. 0 = No Sound Blaster interrupt.

Hardware Volume Control   **(Maestro_Base+1Bh, R/W)**

Reserved							Split
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:1	--	Reserved.
0	Split	Hardware volume/counter control register split. 1 = Split volume register from counter register. 0 = Do not split volume from counter register.

Shadow of Mixer
Register for Voice   **(Maestro_Base+1Ch, R/W)**

Voice Vol. Left			HWML	Voice Vol. Right			HWMR
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:5	VVL	Voice Volume Left.
4	HWML	Hardware Volume Mute Left. 1 = mute
3:1	VVR	Voice Volume Right

Bits	Name	Description
0	HWMR	Hardware Volume Mute Right. 1 = mute

HW Volume Control
Counter for Voice   **(Maestro_Base+1Dh, R/W)**

Voice Vol. Left			HWML	Voice Vol. Right			HWMR
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:5	VVL	Voice Volume Left.
4	HWML	Hardware Volume Mute Left. 1 = mute
3:1	VVR	Voice Volume Right
0	HWMR	Hardware Volume Mute Right. 1 = mute

Shadow of Mixer
Register for Master   **(Maestro_Base+1Eh, R/W)**

Master Vol. Left			HWML	Master Vol. Right			HWMR
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:5	MVL	Master Volume Left.
4	HWML	Hardware Master Mute Left. 1 = mute
3:1	MVR	Master Volume Right
0	HWMR	Hardware Master Mute Right. 1 = mute

HW Volume Control
Counter for Master   **(Maestro_Base+1Fh, R/W)**

Master Vol. Left			HWML	Master Vol. Right			HWMR
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:5	MVL	Master Volume Left.
4	HWML	Hardware Master Mute Left. 1 = mute
3:1	MVR	Master Volume Right
0	HWMR	Hardware Master Mute Right. 1 = mute

1983 MAESTRO-3I DATA SHEET

Game Port Control Registers

Joystick 1 X-Delay (Maestro_Base+20h,+21h, R/W)

2A	2B	1A	1B	Delay											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:12	2A/2B 1A/1B	Fire buttons.
11:0	Delay[11:0]	Timer delay in units of 2 microseconds.

Joystick 1 Y-Delay (Maestro_Base+24h,+25h, R/W)

2A	2B	1A	1B	Delay											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:12	2A/2B 1A/1B	Fire buttons.
11:0	Delay[11:0]	Timer delay in units of 2 microseconds.

Joystick 2 X-Delay (Maestro_Base+28h,+29h, R/W)

2A	2B	1A	1B	Delay											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:12	2A/2B 1A/1B	Fire buttons.
11:0	Delay[11:0]	Timer delay in units of 2 microseconds.

Joystick 2 Y-Delay (Maestro_Base+2Ch,+2Dh, R/W)

2A	2B	1A	1B	Delay											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:12	2A/2B 1A/1B	Fire buttons.
11:0	Delay[11:0]	Timer delay in units of 2 microseconds.

Codec Control Registers

CODEC Command / Status (Maestro_Base+30h, W)

RW	AD						
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	RW	Read/Write. 1 = Read cycle. 0 = Write cycle (write twice).
6:0	AD[6:0]	CODEC register address.

CODEC Command / Status (Maestro_Base+30h, R)

0	0	0	0	0	0	0	ST
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:1	–	Reserved. Always read 0.
0	ST	Read/write status. 1 = CODEC register read/write is in progress. 0 = CODEC register read/write is done.

CODEC Write Data (Maestro_Base+32h,+33h, W)

WT CODEC Data															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	WT	16 bits of data to be written to the CODEC.

CODEC Read Data (Maestro_Base+32h,+33h, R)

RD CODEC Data															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	RD	16 bits of data read from the CODEC.

Serial Bus Control Registers

Serial Bus Control A   (Maestro_Base+36h,+37h, R/W)

I²S	INS	EIO	ES	PAC SDFS	PAC PME	SAC SDFS	SAC PME	Reserved
15	14	13	12	11	10	9	8	7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15	I²S	I²S input enable. 1 = Enable I²S input. 0 = Disable I²S input.
14	INS	Interleave samples in I/O SRAM enable. 1 = Enable. 0 = Disable.
13	EIO	EN_IOSRAM. I/O SRAM enable. 1 = Enable I/O SRAM. 0 = Disable I/O SRAM.
12	ES	Serial AC-link enable. 1 = Enable serial AC-link. 0 = Disable serial AC-link.
11	PAC SDFS	Driving SDFS of primary AC-link enable. 1 = Enable driving SDFS of primary AC-link. 0 = Disable driving SDFS of primary AC-link.
10	PAC PME	Driving PME from SDI of primary AC-link. 1 = Enable driving PME from SDI of primary AC-link. 0 = Disable driving PME from SDI of primary AC-link.
9	SAC SDFS	Driving SDFS of secondary AC-link enable. 1 = Enable driving SDFS of secondary AC-link. 0 = Disable driving SDFS of secondary AC-link.
8	SAC PME	Driving PME from SDI of secondary AC-link. 1 = Enable driving PME from SDI of secondary AC-link. 0 = Disable driving PME from SDI of secondary AC-link.
7:0	–	Reserved.

Serial Bus Control B   (Maestro_Base+38h, R/W)

I2SEN	SBIF	CDC2	SPDIF	MSS	–	CDC ID
7	6	5	4	3	2	1 0

Bit Definitions:

Bits	Name	Description
7	I2SEN	I²S Dock Enable. 1 = Enable I²S docking interface. 0 = Disable I²S docking interface.
6	SBIF	1 = Enable Sound Blaster interface to ASSP. 0 = Disable Sound Blaster interface to ASSP.

Bits	Name	Description
5	CDC2	1 = Enable secondary AC-link. 0 = Disable secondary AC-link.
4	SPDIF	1 = Enable S/PDIF function. 0 = Disable S/PDIF function.
3	MSS	Modem Slot Select Enable 1 = Select MC97_DI for modem slot. 0 = Select SDI1 for modem slot.
2	–	Reserved.
1:0	CDC ID	Second CODEC ID.

Bit 1	Bit 0	CODEC ID
0	0	AC-Link 1.
0	1	AC-Link 2.
1	0	Reserved.
1	1	MC98/MC97.

Serial Bus Control C   (Maestro_Base+39h, R/W)

–	PMS2	PMS1	Reserved				
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7	–	Reserved.
6	PMS2	Status bit of PME# assertion from SDI2.
5	PMS1	Status bit of PME# assertion from SDI1.
4:0	–	Reserved.

SDO Output
Destination Control   (Maestro_Base+3Ah, R/W)

I/O	HS	L2DAC	PCM R/LF	PCM CLS	L1DAC	PCM L/R	CA
15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0

Bit Definitions:

Bits	Name	Description
15:14	I/O	I/O control output.

Bit 15	Bit 14	Destination
0	0	Primary
0	1	Secondary
1	0	Mute
1	1	Both

Bits	Name	Description
13:12	HS	Handset output.

Bit 13	Bit 12	Destination
0	0	Primary
0	1	Secondary
1	0	Mute
1	1	Both

Bits	Name	Description
11:10	L2DAC	Line 2 DAC output.

Bit 11	Bit 10	Destination
0	0	Primary
0	1	Secondary
1	0	Mute
1	1	Both

Bits	Name	Description
9:8	PCM R/LF	PCM R_SURR/LFE output.

Bit 9	Bit 8	Destination
0	0	Primary
0	1	Secondary
1	0	Mute
1	1	Both

Bits	Name	Description
7:6	PCM CLS	PCM Center/L_SURR output.

Bit 7	Bit 6	Destination
0	0	Primary
0	1	Secondary
1	0	Mute
1	1	Both

Bits	Name	Description
5:4	L1DAC	Line 1 DAC output.

Bit 5	Bit 4	Destination
0	0	Primary
0	1	Secondary
1	0	Mute
1	1	Both

Bits	Name	Description
3:2	PCM L/R	PCM L/R output.

Bit 3	Bit 2	Destination
0	0	Primary
0	1	Secondary
1	0	Mute
1	1	Both

Bits	Name	Description
1:0	CA	Command address output.

Bit 1	Bit 0	Destination
0	0	Primary
0	1	Secondary
1	0	MC Codec
1	1	Reserved

SDI Input Destination Control (Maestro_Base+3Ch, R/W)

I/O		HS		L2ADC		–		MIC ADC		L1ADC		PCM L/R		SA	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:14	I/O	I/O status input.

Bit 15	Bit 14	Destination
x	0	Primary
x	1	Secondary

Bits	Name	Description
13:12	HS	Handset input.

Bit 13	Bit 12	Destination
0	0	Primary
0	1	Secondary
1	x	Mute both

Bits	Name	Description
11:10	L2ADC	Line 2 DAC input.

Bit 11	Bit 10	Destination
0	0	Primary
0	1	Secondary
1	x	Mute both

Bits	Name	Description
9:8	–	Reserved.

Bits	Name	Description
7:6	MIC ADC	MIC ADC input.

Bit 7	Bit 6	Destination
x	0	Primary
x	1	Secondary

Bits	Name	Description
5:4	L1ADC	Line 1 ADC input.

Bit 5	Bit 4	Destination
0	0	Primary
0	1	Secondary
1	x	Mute both

Bits	Name	Description
3:2	PCM L/R	PCM L/R input.

Bit 3	Bit 2	Destination
0	0	Primary
0	1	Secondary
1	0	Reserved
1	1	Both

Bits	Name	Description
1:0	SA	Status address/data input.

Bit 1	Bit 0	Destination
0	0	Primary
0	1	Secondary
1	0	MC Codec
1	1	Reserved

S/PDIF Input Control (Maestro_Base+3h, R/W)

SPIF				Reserved	SPID	Reserved	SPIE
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:4	SPIF	SPDIF input data frequency (read-only) 00h = 44.1 kHz 02h = 48 kHz 03h = 32 kHz
3	–	Reserved.
2	SPID	SPDIF input data format 1 = not supported 0 = PCM data format
1	–	Reserved
0	SPIE	SPDIF Input Enable 1 = Enable SPDIF input 0 = Disable SPDIF input

Modem Wakeup
Control   (Maestro_Base+40h,+41h, R/W)

Reserved	VAUXD	Reserved	SIL	R	PMG_RI	Reserved
15 14 13 12	11	10 9 8 7	6	5	4	3 2 1 0

Bit Definitions:

Bits	Name	Description
15:12	–	Reserved.
11	VAUXD	VAUX Detect status bit
10:7	–	Reserved.
6	SIL	SiLab DAA Enable. 1 = Enable SiLab DAA support. 0 = Disable SiLab DAA support.
5	–	Reserved.
4	PMG_RI	1 = Enable PME# generation from ring input.
3:0	–	Reserved

Modem Ring
Input Status   (Maestro_Base+42h,+43h, R/W)

Reserved	RIS	–
15 14 13 12 11 10 9 8 7 6 5 4 3	2	1 0

Bit Definitions:

Bits	Name	Description
15:3	–	Reserved.
2	RIS	Ring Input Status Read for ring input status. 1 = Indicates ring input is pulsing. 0 = Ring input is idle. Write 1 to clear the status bit.
1:0	–	Reserved.

Time Stamp 0 for Ring   (Maestro_Base+4Ah,+4Bh, R)

TS0_RI
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:0	TS0_RI	Time stamp 0 for Ring.

Time Stamp 1 for Ring   (Maestro_Base+4Ch,+4Dh, R)

TS1_RI
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:0	TS1_RI	Time stamp 1 for Ring.

DAA Data
Input / Output Port   (Maestro_Base+50h,+51h, R/W)

DAA Data I/O	RI#
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	0

Bit Definitions:

Bits	Name	Description
15:1	DDI/O	DAA data input/output to MC'97.
0.	RI#	Ring data input from MC'97.

GPIO Registers

GPIO Data   (Maestro_Base+60h, +61h, R/W)

GPIO data
15   14   13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:0	GPD	GPIO data.

GPIO Mask   (Maestro_Base+64h, +65h, R/W)

GPIO write mask
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:0	GPWM	GPIO write mask. 1 = Mask write. 0 = Unmask write.

GPIO Direction   (Maestro_Base+68h, +69h, R/W)

GPIO direction
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Bit Definitions:

Bits	Name	Description
15:0	GPD	GPIO direction. 1 = Output. 0 = Input (default). Note: GPIO15 is OUTPUT only; bit 15 of this register is ignored).

EEPROM Data Port   (Maestro_Base+6Ch,+6Dh R/W)

Reserved	ES	EK	EO	EI
15 14 13 12 11 10 9 8 7 6 5 4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:4	–	Reserved
3	ES	ECS output to EEPROM.

Bits	Name	Description
2	EK	ECLK output to EEPROM.
1	EO	EDO output to EEPROM.
0	EI	EDI input from EEPROM.

ASSP Memory Control Registers

ASSP Memory / Index Port   (Maestro_Base+80h,+81h, R/W)

ASSP memory/index															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:0	AM/I	Host-to-ASSP 16-bit memory index port. Points to 64K word of ASSP memory.

ASSP Memory Port   (Maestro_Base+82h,+83h, R/W)

Reserved														MSS	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:2	–	Reserved.
1:0	MSS	DMA memory space selection.

Bit 1	Bit 0	Memory Space
0	x	Reserved
1	0	ASSP program memory
1	1	ASSP data memory

ASSP Data Port   (Maestro_Base+84h,+85h, R/W)

ASSP data															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Each time this register is accessed for a read or write, the ASSP Memory/Index port (Maestro_Base+80h, +81h) is incremented by 1. The index port is 4K word paged.

Bit Definitions:

Bits	Name	Description
15:0	AD	16-bit data (word) port.

Game Port Address Registers

Game Port Address A   (Maestro_Base+90h, R/W)

Native address port for game port							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 200h.

Game Port Address B   (Maestro_Base+91h, R/W)

Native address port for game port							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 201h.

Game Port Address C   (Maestro_Base+92h, R/W)

Native address port for game port							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 202h.

Game Port Address D   (Maestro_Base+93h, R/W)

Native address port for game port							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 203h.

Game Port Address E   (Maestro_Base+94h, R/W)

Native address port for game port							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 204h.

Game Port Address F   (Maestro_Base+95h, R/W)

Native address port for game port							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 205h.

Game Port Address G   (Maestro_Base+96h, R/W)

Native address port for game port							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 206h.

Game Port Address H   (Maestro_Base+97h, R/W)

Native address port for game port							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAGP	Native address port for game port. Alias I/O port for 207h.

MPU-401 Address Registers

MPU-401 Port Address A   (Maestro_Base+98h, R/W)

Native address port for MPU-401							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAMPU	Native address port for MPU-401. Alias I/O port for 330h.

MPU-401 Port Address B   (Maestro_Base+99h, R/W)

Native address port for MPU-401							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAMPU	Native address port for MPU-401. Alias I/O port for 331h.

MPU-401 Port Address C   (Maestro_Base+9Ah, R/W)

Native address port for MPU-401							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAMPU	Native address port for MPU-401. Alias I/O port for 330h.

MPU-401 Port Address D   (Maestro_Base+9Bh, R/W)

Native address port for MPU-401							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	NAMPU	Native address port for MPU-401. Alias I/O port for 331h.

Clock Multiplier
Data Port A   (Maestro_Base+9Ch, +9Dh, R)

–						4xS					3xS				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
15:10	–	Reserved.
9:5	4xS	x4 counter status.
4:0	3xS	x3 counter status.

ASSP Clock Control Registers

ASSP Control A   (Maestro_Base+A2h, R/W)

Reserved	36CLK	Reserved		33/49CLK	Reserved	0WS
7	6	5	4	3	2 1	0

Bit Definitions:

Bits	Name	Description
7	–	Reserved.
6	36CLK	36 MHz DSP clock select. 1 = Select 36 MHz DSP clock. Note: Enable PCI config register 53h bit 7 before enabling bit 6.
5:4	–	Reserved.
3	33/49 CLK	33 MHz or 49.152 MHz ASSP clock select. 1 = Enable 49.152 MHz ASSP clock. 0 = Enable 33 MHz ASSP clock.
2:1	–	Reserved.
0	0WS	ASSP 0-wait state enable. 1 = Enable ASSP 0-wait state. 0 = Disable ASSP 0-wait state.

NOTE: When both bit 6 and bit 3 are enabled, 49.152 MHz ASSP clock is selected

ASSP Control B   (Maestro_Base+A4h, R/W)

Reserved			CRE	Reserved			ARST
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:5	--	Reserved.
4	CRE	Clock run/enable. 1 = Stop ASSP clock. 0 = Enable ASSP clock.
3:1	–	Reserved.
0	ARST	ASSP reset/run. 1 = Run ASSP. 0 = Reset ASSP.

ASSP Control C   (Maestro_Base+A6h, R/W)

Reserved						EDFM	AHIR
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:2	--	Reserved.
1	EDFM	FM address remapping. 1 = Disable FM address remapping. 0 = Enable FM address remapping.
0	AHIR	ASSP to host interrupt request. 1 = Enable ASSP to host IRQ. 0 = Disable ASSP to host IRQ.

ASSP to Host IRQ Status   (Maestro_Base+ACh, R/W)

ASSP IRQ status							
7	6	5	4	3	2	1	0

Bit Definitions:

Bits	Name	Description
7:0	AIS	ASSP to host software interrupt request status. Read for pending interrupt status. 1 = Interrupt pending. 0 = No interrupt pending. Write 1 to clear pending interrupt request. The bits in this register are set to 1 by ASSP to request interrupts from the host.

ASSP DMA Registers

Host Memory End
Address (Low Word)   (ASSPIO_4000h, R/W)

Host Memory End Address (Low Word)															R
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register corresponds to the PCI address [15:1].

Bits Definitions:

Bits	Name	Description
15:1	HMEA (L)	Host Memory End Address (Low Word).
0	--	Reserved. Always 0s.

Host Memory End
Address (High Word)   (ASSPIO_4001h, R/W)

Reserved				Host Memory End Address (High Word)											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

This register corresponds to the PCI address [27:16].

Bits Definitions:

Bits	Name	Description
15:12	–	Reserved. Always write 0s and read back as 0s.
11:0	HMEA (H)	Host Memory End Address (High Word).

ASSP Data Memory
End Address   (ASSPIO_4002h, RW)

ASSP Data Memory End Address															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bits Definitions:

Bits	Name	Description
15:0	ADMA	ASSP Data Memory End Address.

Host Memory Starting Address/
Current Pointer (Low Word)   (ASSPIO_4003h, R/W)

Host Memory Address/Pointer (Low Word)															R
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

When this register is written to by the ASSP, it means host memory starting address. This register corresponds to PCI address [15:1].

Bits Definitions:

Bits	Name	Description
15:1	HMSA (L)	Host Memory Starting Address (Low Word).
0	--	Reserved. Always write 0s.

When this register is read from by the ASSP, it means current host address pointer. The pointer is updated after each data transfer.

Bits Definitions:

Bits	Name	Description
15:1	–	Current host address pointer.
0	–	Reserved. Always read back as 0s.

Host Memory Starting Address/
Current Pointer (High Word) (ASSPIO_4004h, R/W)

Reserved				Host Memory Starting Address (High Word)											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

When this register is written to by the ASSP, it means host memory starting address. This register corresponds to PCI address [27:16].

Bits Definitions:

Bits	Name	Description
15:12	–	Reserved. Always write 0s.
11:0	HMSA (H)	Host Memory Starting Address (High Word).

When this register is read from by the ASSP, it means current host address pointer. The pointer is updated after each data transfer.

Bits Definitions:

Bits	Name	Description
15:12	–	Reserved. Always write 0s.
11:0	CHAP	Current host address pointer (corresponding to PCI address [27:16]).

ASSP Data Memory Starting
Address/Current Pointer (ASSPIO_4005h, R/W)

ASSP Data Memory Address/Pointer															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

When this register is written to by the ASSP, it means ASSP data memory starting address.

Bits Definitions:

Bits	Name	Description
15:0	DDMS	ASSP Data Memory Starting Address.

When this register is read from by the ASSP, it means ASSP data memory address pointer. The pointer is updated after each data transfer.

Bits	Name	Description
15:0	DDMP	ASSP data memory address pointer.

DMA Control (ASSPIO_4006h, R/W)
(Write)

Reserved				AMEAS	HMEAS	XBINT	R/W	DMACTRL							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

(Read)

Reserved				AMEAS	HMEAS	HMBS	R/W	XFERCNT							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

When this register is written to by the ASSP, host and data memory reads and writes are being monitored. Hardware interrupts are generated as necessary if the address counter crosses the host memory 64K boundary and bit 9 will be set to 1 accordingly.

Bits 10 and 11 are read-only and return host and ASSP data memory end address status when read. Four mechanisms will cause the ASSP DMA hardware interrupt to be generated.

1. Completion of data transfer (I/O 4006, bit 12 = 1).
2. The host memory end address has been reached (I/O 4006, bit 10 = 1).
3. The ASSP memory end address has been reached (I/O 4006, bit 11 = 1).
4. The host memory 64K boundary has been crossed (I/O 4006, bit 9 = 1).

Bits Definitions (Write):

Bits	Name	Description
15:10	–	Reserved. Always write 0s
9	XBINT	Host memory crossing 64K Boundary Interrupt Enable. 1 = Enable. 0 = Disable.
8	R/W	ASSP Host Memory Read/Write Enable. 1 = Read ASSP data memory and write host memory. 0 = Read host memory and write ASSP data memory.
7:0	DMA CTRL	Word transfer counts for one-time DMA kick-off from 1 to 256 words (00h - FFh).

When this register is read from by the ASSP, it means ASSP data memory address pointer. The pointer is updated after each data transfer.

Bits Definitions (Read):

Bits	Name	Description
15:13	--	Reserved. Always write 0s.
12	XFER STAT	Transfer Counter Status. 1 = ASSP transfer counter reached (read-only) 0 = ASSP transfer counter not reached.
11	AMEAS	ASSP Memory End Address Status (read-only). 1 = ASSP memory end address reached. 0 = ASSP memory end address not reached.

Bits	Name	Description
10	HMEAS	Host Memory End Address Status (read-only). 1 = Host memory end address reached. 0 = Host memory end address not reached.
9	HMBS	Host Memory Boundary Status. (read only). 1 = Host memory boundary crossed. 0 = Host memory boundary not crossed.
8	STATUS	ASSP Status. 1 = DMA transfer in progress. 0 = DMA transfer complete.
7:0	XFER CNT	Hold transfer count as written.

ELECTRICAL CHARACTERISTICS

Table 13 Absolute Maximum Ratings

Ratings	Symbol	Value	Units
Digital supply voltage	V_{DD}	-0.3 to 4.5	V
Input voltage	V_{IN}	VDD +0.5	V
Operating temperature range	T_A	0 to 70	°C
Storage temperature range	T_{STG}	-40 to 125	°C

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. There are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

Table 14 DC Operating Condition

Parameter	Definition	Min	Typ	Max	Unit
VDD	Digital supply voltage	3.0	3.3	3.6	V
T_{AMB}	Ambient temperature	0	25	70	°C

Table 15 Digital Characteristics

Parameter	Definition	Min	Typ	Max	Unit
Operating Conditions (V_{DDD} = 3.3 V, T_A = 25 °C) (TTL-Compatible)					
V_{IH}	High-level input voltage	2.0			V
V_{OH}	High-level output voltage	2.4			V
V_{IL}	Low-level input voltage	0		0.8	V
V_{OL}	Low-level output voltage			0.4	V

ES1983 Recommended DC Operating Condition

Table 16 Power Management Characteristics

Operating Mode	Typical	Unit
M3 in D0 state (normal operation)	72	mA
M3 in D1 state	14	mA
M3 in D2 state	14	mA
M3 in D3$_{hot}$ state	6	mA
M3 in D3$_{cold}$ state	0.5	mA

PCI BUS TIMING DIAGRAMS
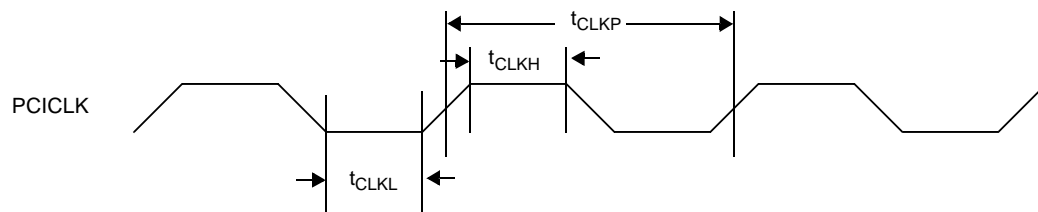
Symbol	Parameter	Min	Typ	Max	Units
t_{CLKP}	PCI bus clock cycle time	30			ns
t_{CLKL}	PCI bus clock low pulse width	11			ns
t_{CLKH}	PCI bus clock high pulse width	11			ns

Figure 8 PCI Clock Timing
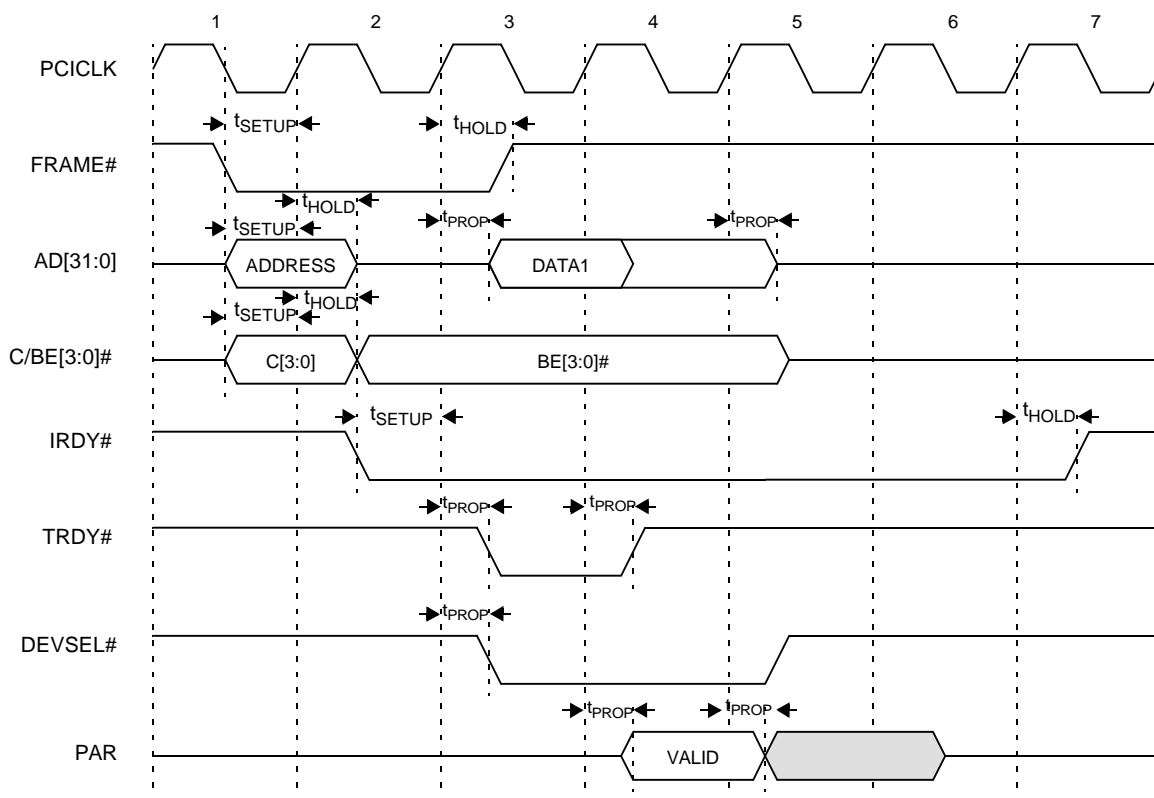
Symbol	Parameter	Min	Typ	Max	Units
t_{SETUP}	Input setup time to PCICLK	7			ns
t_{HOLD}	Input holds time to PCICLK	0			ns
t_{PROP}	Output propagation delay time from PCICLK (0pF load min., 50 pF load max)	2		11	ns

Figure 9 PCI Bus I/O Read Cycle
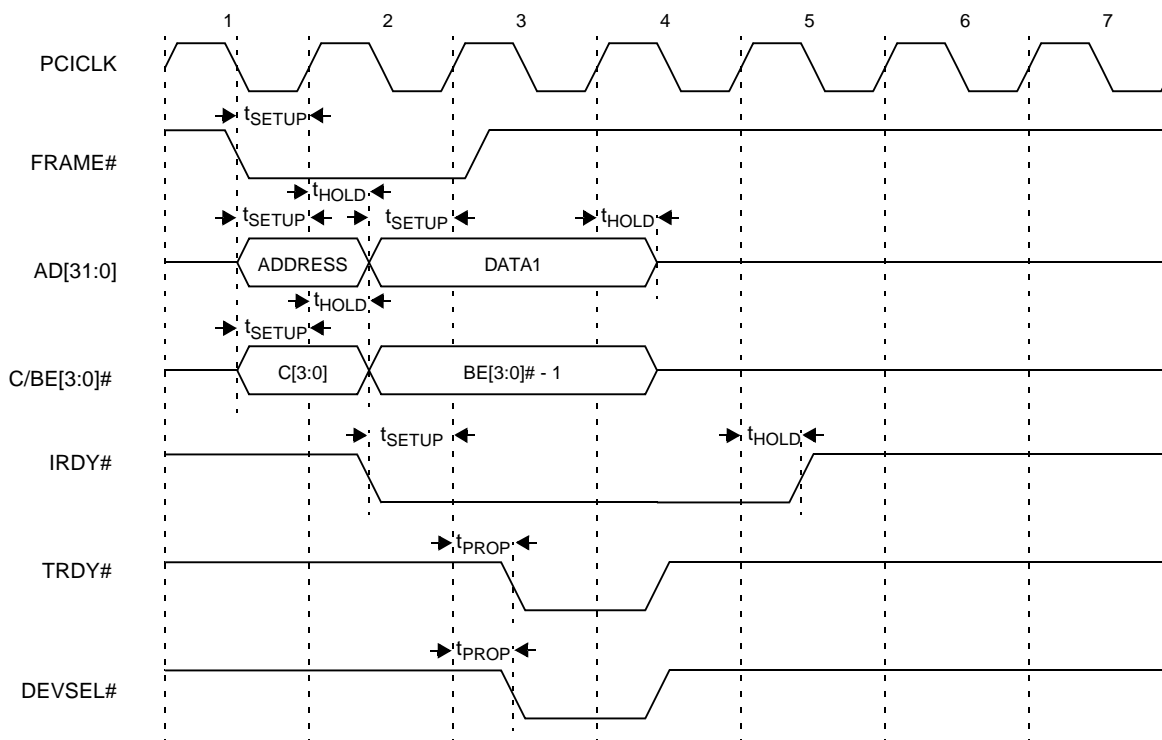
Symbol	Parameter	Min	Typ	Max	Units
t_{SETUP}	Input setup time to PCICLK	7			ns
t_{HOLD}	Input holds time to PCICLK	0			ns
t_{PROP}	Output propagation delay time from PCICLK (0pF load min., 50 pF load max)	2		11	ns

Figure 10 PCI Bus I/O Write Cycle
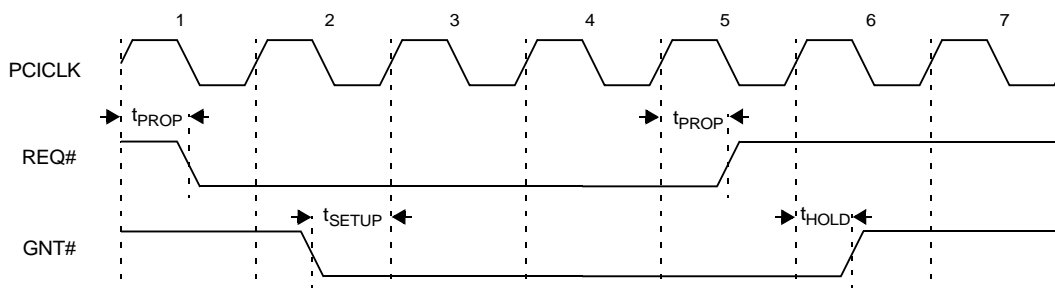
Symbol	Parameter	Min	Typ	Max	Units
t_{SETUP}	Input setup time to PCICLK	7			ns
t_{HOLD}	Input holds time to PCICLK	0			ns
t_{PROP}	Output propagation delay time from PCICLK (0pF load min., 50 pF load max)	2		11	ns

Figure 11 PCI Bus Master Request
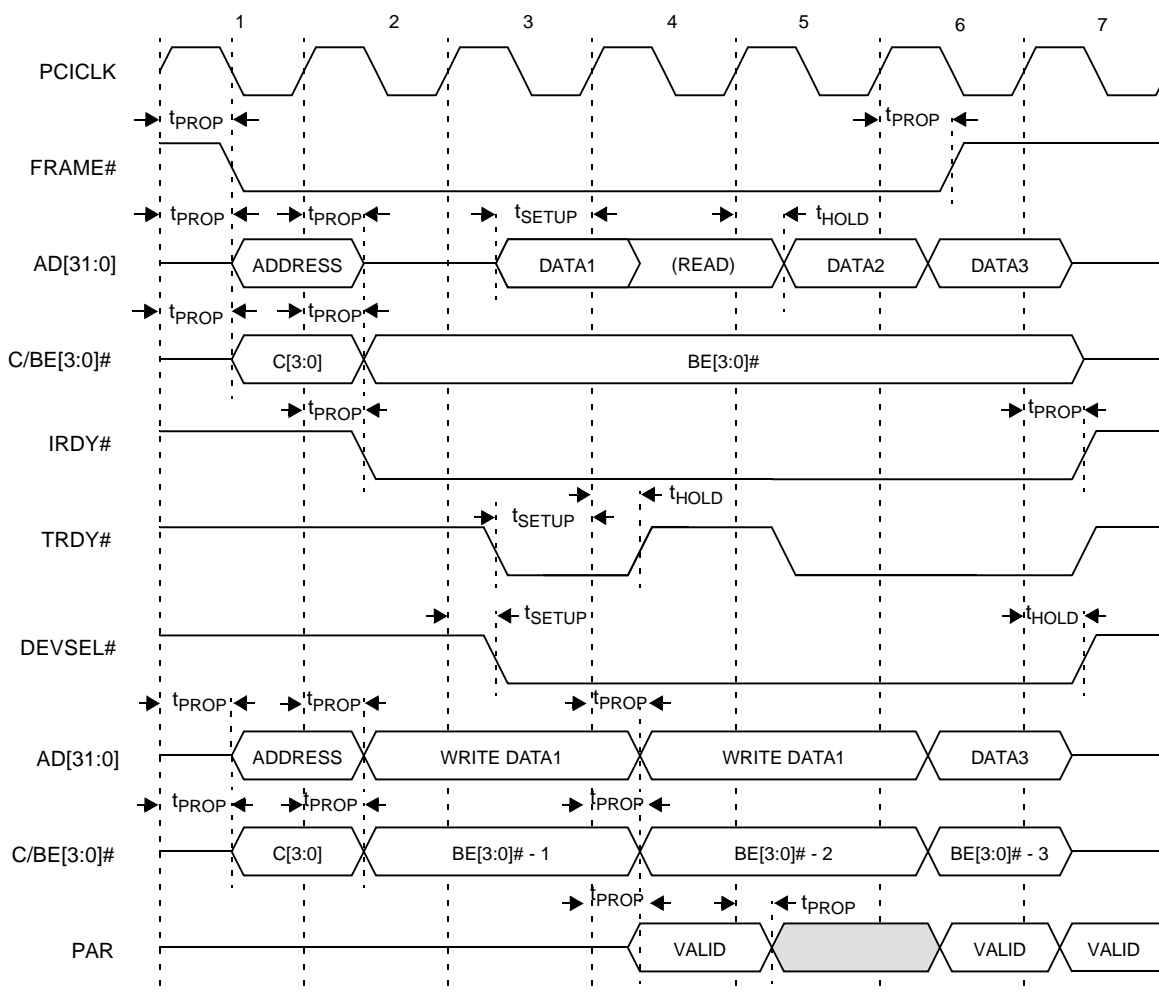
Symbol	Parameter	Min	Typ	Max	Units
t_{SETUP}	Input setup time to PCICLK	7			ns
t_{HOLD}	Input holds time to PCICLK	0			ns
t_{PROP}	Output propagation delay time from PCICLK (0pF load min., 50 pF load max)	2		11	ns

Figure 12 PCI Bus Master Read/Write Cycle

AC-LINK/MC-LINK TIMING DIAGRAMS
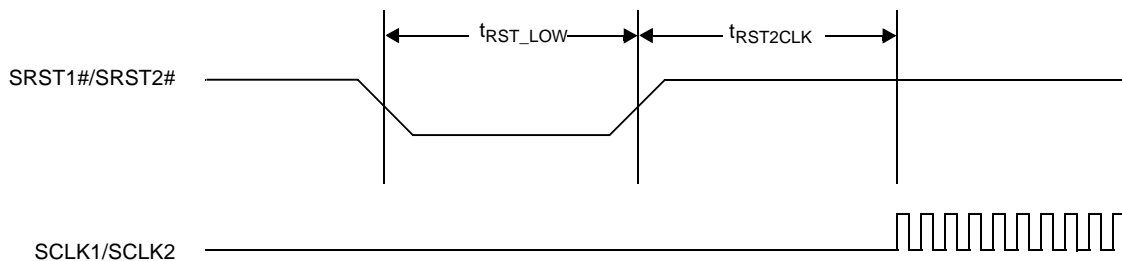
Symbol	Parameter	Min	Typ	Max	Units
t_{RST_LOW}	RESET# active-low pulse width	1.0			µs
$t_{RST2CLK}$	RESET# inactive to BIT_CLK start-up delay	162.8			ns

Figure 13 AC-Link/MC-Link Cold Reset
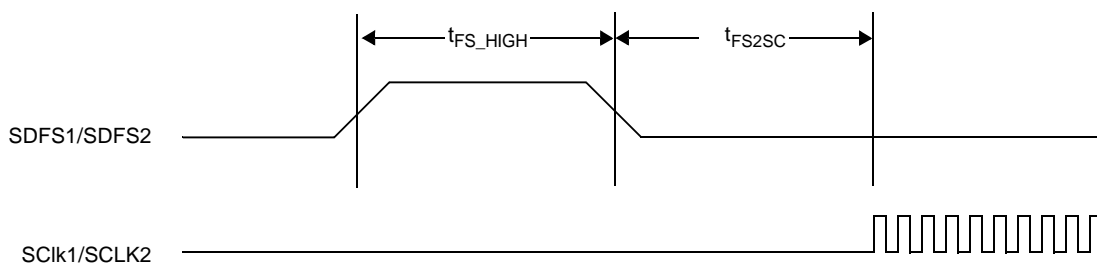
Symbol	Parameter	Min	Typ	Max	Units
t_{FS_HIGH}	SYNC active-high pulse width	1.0			µs
t_{FS2SC}	SYNC inactive to BIT_CLK start-up delay	162.8			ns

Figure 14 AC-Link/MC-Link Warm Reset
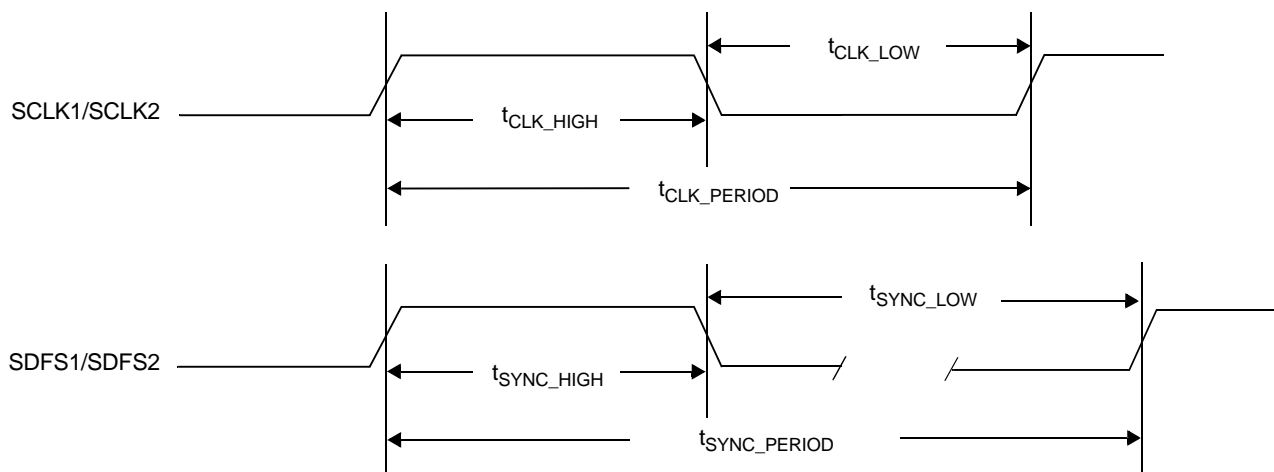
Symbol	Parameter	Min	Typ	Max	Units
	SCLKn frequency		12.288		MHz
t_{CLK_PERIOD}	SCLKn period		81.4		ns
	SCLKn output jitter			750	ps
t_{CLK_HIGH}	SCLKn high pulse width*	36	40.7	45	ns
t_{CLK_LOW}	SCLKn low pulse width*	36	40.7	45	ns
	SDFSn frequency		48.0		kHz
t_{SYNC_PERIOD}	SDFSn period		20.8		µs
t_{SYNC_HIGH}	SDFSn high pulse width		1.3		ns
t_{SYNC_LOW}	SDFSn low pulse width		19.5		ns

* = Worst case duty cycle restricted to 45/55

Figure 15 AC-Link/MC-Link Clocks Timing
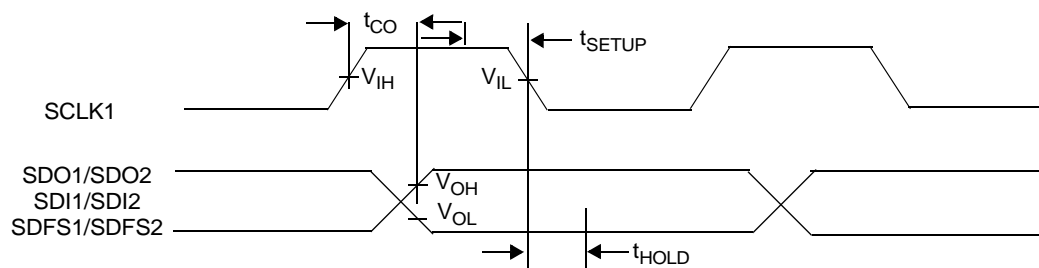
Symbol	Parameter	Min	Typ	Max	Units
	AC-Link Output Valid Delay Timing Parameters				
t_{CO}	Output Valid Delay from rising edge of BIT_CLK			15	ns
	Note 1: Timing is for SDATA and SYNC outputs with respect to BIT_CLK *at the device driving the output*. Note 2: 50 pF external load.				
	AC-Link Input Setup and Hold Timing Parameters				
t_{SETUP}	Input Setup to falling edge of BIT_CLK	10			ns
t_{HOLD}	Input Hold to falling edge of BIT_CLK	10			ns
	AC-Link Combined Rise or Fall Plus Flight Timing Parameters				
	BIT_CLK combined rise or fall plus flight time (Primary Codec to Controller or Secondary)			7	ns
	SDATA combined rise or fall plus flight time (Output to Input)			7	ns
	Note: Combined rise or fall plus flight times are provided for worst case scenario modeling purposes.				

Figure 16 AC-Link Data Output and Input Timing Diagram
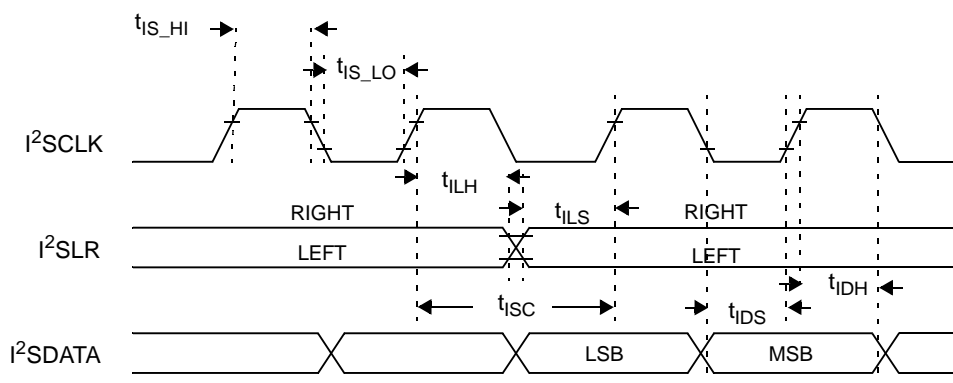
Symbol	Parameter	Min	Typ	Max	Units
t_{ISC}	I^{2}SCLK cycle time	54			ns
t_{IS_HI}	I^{2}SCLK HIGH time	15			ns
t_{IS_LO}	I^{2}SCLK LOW time	15			ns
t_{IDS}	I^{2}DATA setup time	12			ns
t_{IDH}	I^{2}DATA hold time	2			ns
t_{ILS}	I^{2}SLR setup time	12			ns
t_{ILH}	I^{2}SLR hold time	2			ns

Figure 17 I^{2}S Port Timing
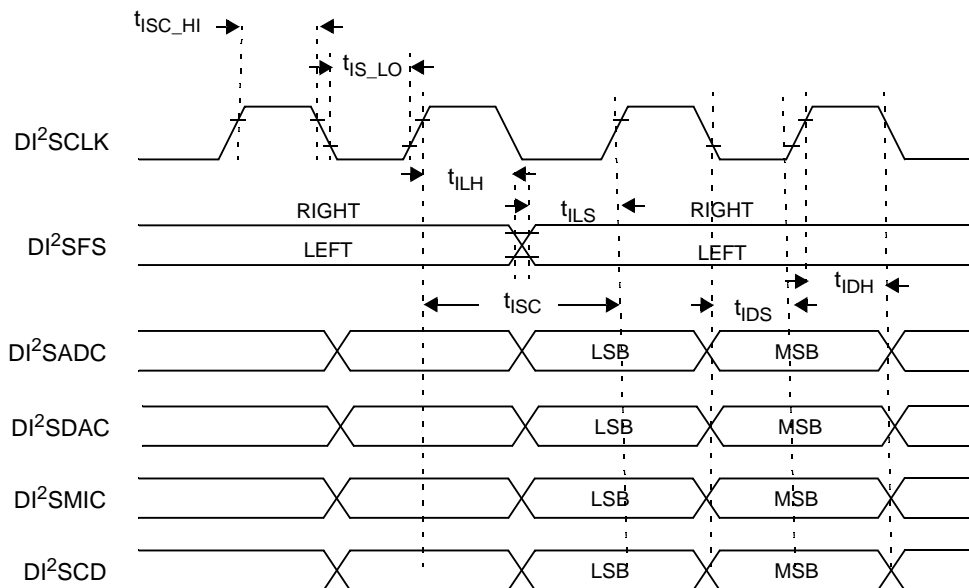
Symbol	Parameter	Min	Typ	Max	Units
t_{ISC}	DI^{2}SCLK cycle time		325		ns
t_{IS_HI}	DI^{2}SCLK HIGH time	140			ns
t_{IS_LO}	DI^{2}SCLK LOW time	140			ns
t_{ILS}	DI^{2}SFS setup time	140			ns
t_{ILH}	DI^{2}SFS hold time	150			ns
t_{IDS}	DI^{2}SADC setup time	15			ns
t_{IDH}	DI^{2}SADC hold time	15			ns
t_{IDS}	DI^{2}SDAC setup time	140			ns
t_{IDH}	DI^{2}SDAC hold time	150			ns
t_{IDS}	DI^{2}SMIC setup time	15			ns
t_{IDH}	DI^{2}SMIC hold time	15			ns
t_{IDS}	DI^{2}SCD setup time	15			ns
t_{IDH}	DI^{2}SCD hold time	15			ns

Figure 18 I^{2}S Docking Link Timing
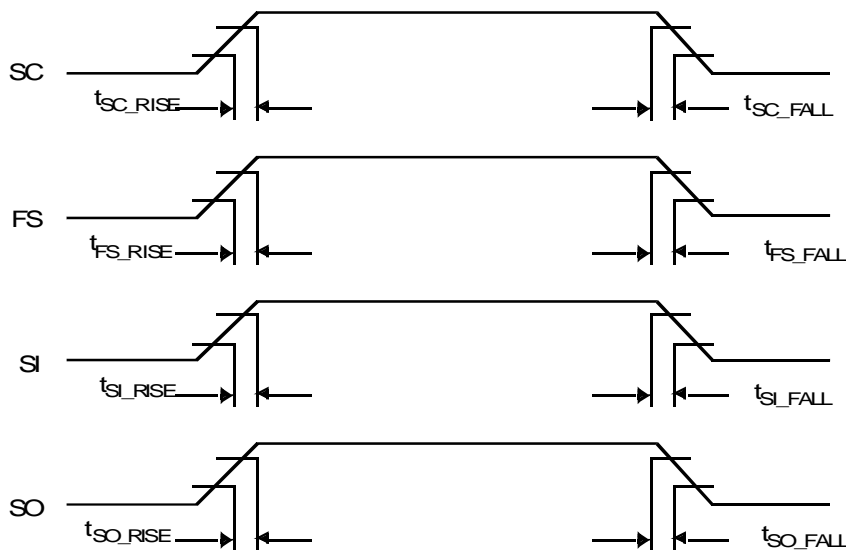
Symbol	Parameter	Min	Typ	Max	Units
t_{SC_RISE}	SCLCKn rise time	2		6	ns
t_{SC_FALL}	SCLKn fall time	2		6	ns
t_{FS_RISE}	SDFSn rise time	2		6	ns
t_{FS_FALL}	SDFSn fall time	2		6	ns
t_{SI_RISE}	SDIn rise time	2		6	ns
t_{SI_FALL}	SDIn fall time	2		6	ns
t_{SO_RISE}	SDOn rise time	2		6	ns
t_{SO_FALL}	SDOn fall time	2		6	ns

Figure 19 AC-Link Signal Rise and Fall Times
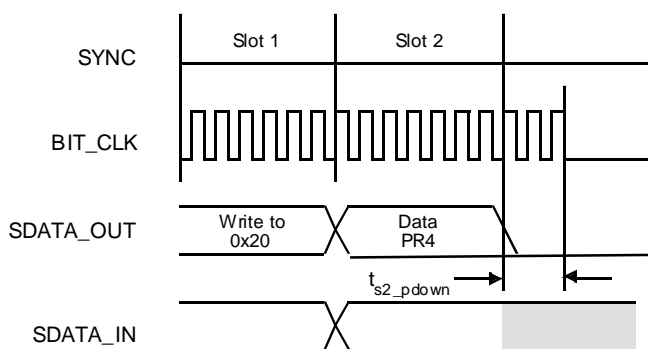
Note: BIT_CLK not to scale.

Symbol	Parameter	Min	Typ	Max	Units
t_{S2_PDOWN}	End of Slot 2 to BIT_CLK, SDATA_IN low			1.0	µs

Figure 20 AC-Link Low Power Mode Timing

MECHANICAL DIMENSIONS
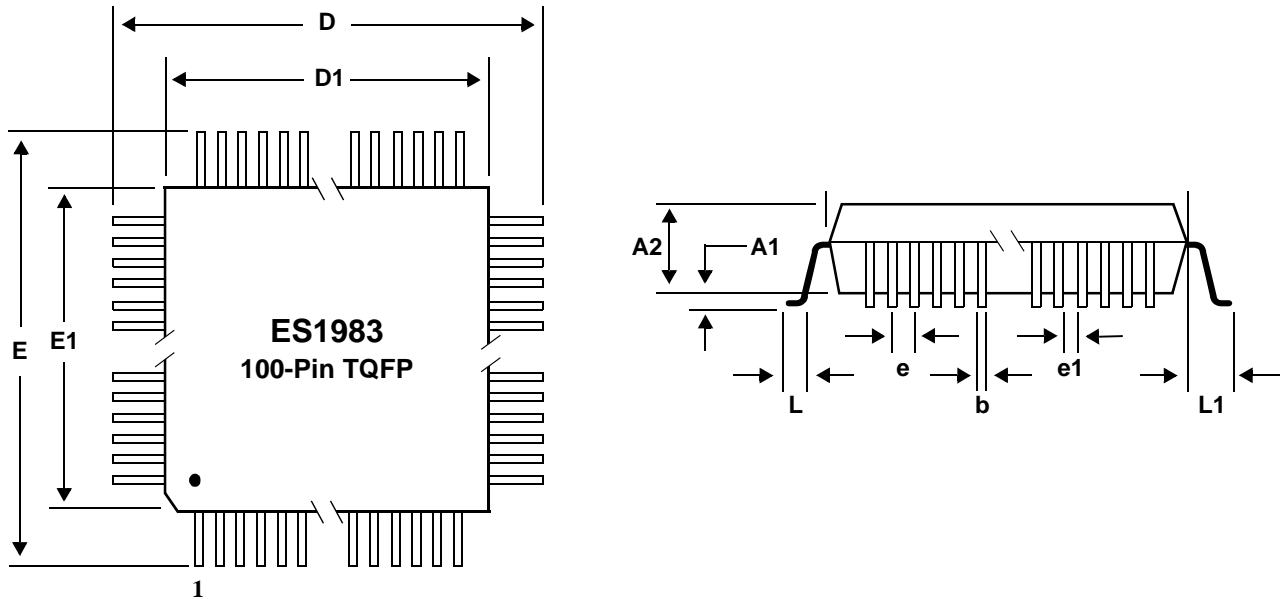
Symbol	Description	Millimeters		
		Min	Nom	Max
D	Lead to lead, X-axis	15.75	16.00	16.25
D1	Package's outside, X-axis	13.90	14.00	14.10
E	Lead to lead, Y-axis	15.75	16.00	16.25
E1	Package's outside, Y-axis	13.90	14.00	14.10
A1	Board standoff	0.05	0.10	0.15
A2	Package thickness	1.35	1.40	1.45
b	Lead width	0.17	0.22	0.27
e	Lead pitch	-	0.50	-
e1	Lead gap	0.24	-	-
L	Foot length	0.45	0.60	0.75
L1	Lead length	0.93	1.00	1.07
-	Foot angle	0°		7°
-	Coplanarity	-	-	0.102
-	Leads in X-axis	-	25	-
-	Leads in Y-axis	-	25	-
-	Total leads	-	100	-
-	Package type	-	TQFP	-

Figure 21 Mechanical Dimensions

AMR/MDC LAYOUT GUIDELINES

Desktop, notebook, pen-based and PDA portable computers have the following similarities in PCB layout design for audio-modem riser (AMR) cards and audio-modem mobile daughter cards (MDCs):

1. Multi-layer (usually 2 to 4 layer).
2. Double-sided SMT.
3. CPU, core logic (chip set), VGA controller, and system and video memory reside on the same PCB.

This is a very noisy environment for adding an audio-modem subsystem. The following are the guidelines for PCB layout for an ESS-based audio-modem subsystem application in both AMR and MDC cards.

AMR Design Considerations

According to the Intel Audio/Modem Riser Specification, designing an audio-modem subsystem on the motherboard has been problematic at best, primarily due to FCC and international telecomm certification processes that delay the introduction of a motherboard.

From a design standpoint, the audio circuit-related components, including the audio I/O jacks and audio connector must be grouped in the same area in order to help fully realize the full signal-to-noise ratio offered by today's audio Codecs. Modem components affected by the homologation issue include the modem AFE, DAA circuitry and RJ-11 jacks.
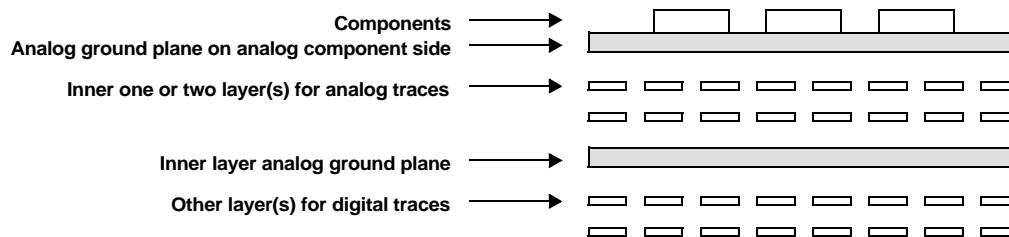
Case A:

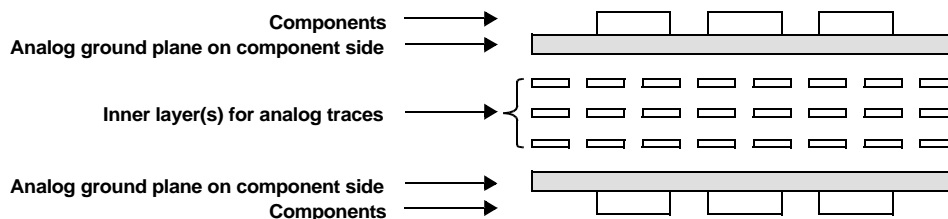Figure 22 Analog Components on One Side of the PCB

Case B:

Figure 23 Analog Components on Both Sides of the PCB.

According to the Intel Audio/Modem Riser Specification, physically partitioning the audio-modem system onto a separate riser module allows the motherboard development cycle to be freed from any delays that might otherwise be associated with the certification process.

Analog Ground Plane

Audio circuits require two layers of analog ground planes for use as shielding for all analog traces. In component placement case A (Figure 22), the first layer of analog ground plane is on the analog component side, the second analog ground plane is on the inner layer, and the analog traces are embedded between these two planes. In component placement case B (Figure 23), the analog ground planes are on both sides of the PCB, and the analog traces are shielded in the middle. The analog traces should be placed as short as possible. The MIC-IN circuit is the most sensitive of the audio circuits, and requires proper and complete shielding.

Ground Isolation

Both the Intel Audio/Modem Riser Specification and the Intel Mobile Audio/Modem Daughter Card Specification recommend using ground isolation techniques in card design to improve the separation of digital noise from the analog sections of a circuit board. Pin B2 on the NLX, ATX and microATX interface connector is the current ground pin to use, according to the AMR specification. For MDC cards, the analog signal ground returns for MONO_PHONE and PC_BEEP/MONO_OUT are used,

according to the MDC specification. For complete details on designing audio-modem riser cards for the NLX, ATX and microATX motherboards, please refer to the latest versions of the Intel Audio/Modem Riser Specification and the Intel specifications for the applicable motherboard.

MDC Design Considerations

Table 17 describes the power requirements of the audio-modem daughter card as they currently appear in the Intel Mobile Audio/Modem Daughter Card Specification.

Table 18 describes the power requirements of the modem-only daughter card as they currently appear in the Intel Mobile Audio/Modem Daughter Card Specification.

Both the Intel Audio/Modem Riser Specification and the Mobile Audio/Modem Daughter Card Specification impose requirements for the BIOS and software drivers, with the vendor being responsible for development of all drivers and BIOS code needed to configure and manage all of the applicable subsystem's hardware resources.

With respect to mounting the RJ-11 telephone jack on the MDC, if the jack is not mounted on the MDC itself, then the surge protection circuitry must be located on the same PCB as the RJ-11 jack, according to the Intel Mobile Audio/Modem Daughter Card Specification. As an alternative, an audio-modem MDC module can house one RJ-11 and three audio mini-jacks.

Please refer to the specification for complete details.

Table 17 Audio-Modem MDC Power Specifications

Power Rail	Min.	Max.	Units	Comments

+3.3V$_{aux/dual}$
 	
Tolerance
 	
Supply Current
   active
   auxiliary
	
	--
	
	--
	--
		
		±5
		
		0.5
		3.0
			
			%
			
			Amps
			mA
				+3.3V$_{aux/dual}$ supply provides auxiliary power when ring detection is necessary, i.e., when the modem is active and when wake-on-ring functionality is desired.
				
				+3.3V$_{aux/dual}$ supply may also optionally provide full power when the modem subsystem is active as per modem subsystem design requirements.

+3.3V
   Tolerance
   Supply Current
	
	--
	--
		
		±5
		0.5
			
			%
			Amps
				+3.3V$_{main}$ supply provides full power when audio and/or modem subsystem is active.

+5V$_{main}$
   Tolerance
   Supply Current
	
	--
	--
		
		±5
		1.5
			
			%
			Amps
				+5V$_{main}$ supply provides full power when audio and/or modem subsystem is active.

Table 18 Modem-Only MDC Power Specifications

Power Rail	Min.	Max.	Units	Comments

+3.3V$_{aux/dual}$
 	
Tolerance
 	
Supply Current
    active
    auxiliary
	--
	
	--
	--
		±5
		
		0.5
		3.0
			%
			
			Amps
			mA
				+3.3V$_{aux/dual}$ supply provides auxiliary power when ring detection is necessary, i.e., when the modem is active and when wake-on-ring functionality is desired.
				
				+3.3V$_{aux/dual}$ supply may also optionally provide full power when the modem subsystem is active as per modem subsystem design requirements.

+3.3V Tolerance Supply Current	-- --	±5 0.5	% Amps	+3.3V$_{main}$ supply provides full power when audio and/or modem subsystem is active.
+5V$_{main}$ Tolerance Supply Current	-- --	±5 0.25	% Amps	+5V$_{main}$ supply provides full power when audio and/or modem subsystem is active.

System Interface

According to the Intel Mobile Audio/Modem Daughter Card Specification, all MDCs use a 30-pin system interface connector between the motherboard and the specific circuitry on the MDC.

Table 19 describes the signal-to-pin interface as published in the Intel Mobile Audio/Modem Daughter Card Specification.

For complete details on the signal types and I/O pins list, refer to the Intel Mobile Audio/Modem Daughter Card Specification. Table 20 describes the MDC-specific system interface electrical specifications as published in the Intel Mobile Audio/Modem Daughter Card Specification. For AC97-specific signals, refer to the Intel Audio Codec '97 Component Specification. For CD_GND specific specifications, refer to the applicable CD-ROM drive specification.

Table 19 MDC System Connector Signal to Pin Interface

Pin	Signal	Pin	Signal
1	MONO_OUT/PC_BEEP	2	AUDIO-PWRDN
3	GND	4	MONO_PHONE
5	AUXA_RIGHT	6	RESERVED
7	AUXA_LEFT	8	GND
9	CD_GND	10	5Vmain
11	CD_RIGHT	12	RESERVED
13	CD_LEFT	14	RESERVED
15	GND	16	RESERVED
17	3.3Vaux/dual	18	RESERVED
19	GND	20	RESERVED
21	3.3Vmain	22	AC97_SYNC
23	AC97_SDATA_OUT	24	AC97_SDATA_IN1
25	AC97_RESET#	26	AC97_SDATA_IN0
27	GND	28	GND
29	AC97_MSTRCLK	30	AC97_BITCLK

Table 20 MDC System Interface Electrical Specifications

Signal Name	Min	Max	Unit

PC_BEEP
    Amplitude
    Source Impedance
    Load Impedance
	0
	2.0
	10
		1.0
		2.5
			V$_{rms}$
			kΩ
			kΩ

MONO_PHONE
    Amplitude
    Load Impedance
	--
	10
		1.0
		--
			V$_{rms}$
			kΩ

MONO_OUT
    Amplitude
    Source Impedance
    Load Impedance
	--
	--
	10
		1.0
		1
		--
			V$_{rms}$
			kΩ
			kΩ

AUDIO_PWRDN
    V$_{IL}$
    V$_{IH}$
	--
	.65 x V$_{DD}$
		.35 x V$_{DD}$
		--
			V
			V

CD_L, CD_R
    Amplitude
    Load Impedance
	1
	10
		--
		--
			V$_{rms}$
			kΩ

Hardware Interface

The Intel Mobile Audio/Modem Daughter Card Specification allows headers or mini-jacks to be used on a combined audio-modem MDC to hook up to the AC'97 part and allows for headers or an RJ-11 jack to hook up to the MC'97 part. A speaker amp and speaker header may be provided for the AC'97 part to enhance the functionality of the audio subsystem.

A headset amp linking the AC'97 part to the header or the mini-jacks is also recommended by the specification. The headset amp provides adequate power to the headset and further drives the audio playback data to the headset speakers.

For modem-only MDC designs, the specification allows for either a header or an RJ-11 jack to hook up with the Tip and Ring portions of the DAA. Refer to the Intel Mobile Audio/Modem Daughter Card Specification for the mechanical dimensions for the audio-modem MDC with jacks and headers.

Notebook Design Considerations

Designing a host-based audio-modem subsystem for a notebook computer requires using the Type III Mini-PCI PC Card form factor and 124-pin system connector. The Type III PC Card is the only card that supports the modem subsystem's Tip and Ring functions, along with the 3.3 V_{AUX} capabilities required by the ACPI specification and CLKRUN#. The Type I and Type II daughter cards and 100-pin system connectors do not support the Tip and Ring functions that an audio-modem subsystem needs to implement the wake-on-ring function.

According to the Mini-PCI Specification, the Type III MDC is intended for very thin profile notebook designs. The Type III card is similar to the Type I in that I/O connectors may be mated to the Type III MDC by a cable and header scheme.

Because there are no current standard motherboard form factors for the notebook or laptop computer platforms, specific placement requirements for the Type III PC Card connector and other component requirements may vary among the specific laptop and notebook computer manufacturers. Contact the specific laptop and notebook computer manufacturer for complete details on motherboards for either laptop or notebook computers as applicable.

Because of its larger pin count and voltage isolation key, designers may choose to connect to modem and local area network interfaces via the system connector and motherboard wiring. Table 21 lists the 124-pin system connector pinout as currently published in the Mini PCI Specification.

Table 21 Type III PC Card System Connector Pinout

Pin	Signal	Pin	Signal
1	TIP	2	RING
	<KEY>		<KEY>
3	LAN RESERVED	4	LAN RESERVED
5	LAN RESERVED	6	LAN RESERVED
7	LAN RESERVED	8	LAN RESERVED
9	LAN RESERVED	10	LAN RESERVED
11	LAN RESERVED	12	LAN RESERVED
13	LAN RESERVED	14	LAN RESERVED
15	LAN RESERVED	16	LAN RESERVED
17	INTB/D#	18	5V
19	3.3V	20	INTA/C#
21	RESERVED	22	RESERVED
23	GROUND	24	3.3V$_{AUX}$
25	CLK	26	RST#
27	GROUND	28	3.3V
29	REQ#	30	GNT#
31	3.3V	32	GROUND
33	AD[31]	34	PME#
35	AD[29]	36	RESERVED
37	GROUND	38	AD[30]
39	AD[27]	40	3.3V
41	AD[25]	42	AD[28]
43	RESERVED	44	AD[26]
45	C/BE[3]#	46	AD[24]
47	AD[23]	48	IDSEL
49	GROUND	50	GROUND
51	AD[21]	52	AD[22]
53	AD[19]	54	AD[20]
55	GROUND	56	PAR
57	AD[17]	58	AD[18]
59	C/BE#[2]	60	AD[16]
61	IRDY#	62	GROUND
63	3.3V	64	FRAME#
65	CLKRUN#	66	TRDY#
67	SERR#	68	STOP#
69	GROUND	70	3.3V
71	PERR#	72	DEVSEL#
73	C/BE#[1]	74	GROUND
75	AD[14]	76	AD[15]
77	GROUND	78	AD[13]

Table 21 Type III PC Card System Connector Pinout

Pin	Signal	Pin	Signal
79	AD[12]	80	AD[11]
81	AD[10]	82	GROUND
83	GROUND	84	AD[09]
85	AD[08]	86	C/BE#[0]
87	AD[07]	88	3.3V
89	3.3V	90	AD[06]
91	AD[05]	92	AD[04]
93	RESERVED	94	AD[02]
95	AD[03]	96	AD[00]
97	5V	98	RESERVED
99	AD[01]	100	SERINT
101	GROUND	102	GROUND
103	AC_SYNC	104	M66EN
105	AC_SDATA_IN1	106	AC_SDATA_OUT
107	AC_BIT_CLK	108	AC_SDATA_IN2
109	AC_CODEC_CLK	110	AC_RESET#
111	MOD_AUDIO_MON	112	RESERVED
113	AUDIO_GND	114	GROUND
115	SYS_AUDIO_OUT	116	SYS_AUDIO_IN
117	SYS_AUDIO_OUT_GND	118	SYS_AUDIO_IN_GND
119	AUDIO_GND	120	AUDIO_GND
121		122	MCPIACT#
123	VCC5A	124	$3.3V_{AUX}$

Audio-Modem Considerations for Wake-On-Ring

In an audio-modem design, the PR4 bit (bit 12) of the Powerdown Control/Status register (index 26h) on an audio Codec controls AC-Link powerdown. As the modem Codec is the secondary Codec in such a design, the MLNK bit becomes meaningless because the audio and modem drivers must be mutually exclusive of each other.

Further, since no standard mechanism exists for the modem driver to know when the audio driver is about to program the audio Codec to PR4 (so the modem driver can set the MLNK bit), the exclusiveness of the drivers becomes mandatory.

In an audio-modem design, the audio driver must leave BIT_CLK on and not shut it off when the modem system is in D0 state. The audio driver must manage only the audio Codec and the modem drive must manage only the modem Codec. No dual device interaction is permitted for either driver as required by the AC'97 Component Specification, Revision 2.1. Instead, the modem Codec, as the secondary Codec, supports an additional V_{AUX} powered clock input when the AC-Link and BIT_CLK is powered off.

Support for Multiple Speaker Configurations

The ES1983 can support designs for mutli-speaker configurations up to a total of six speakers. To do this, additional slots in the AC'97 data I/O frames are utilized.

Slots 3 and 4 are used for standard two-speaker configurations. To configure the ES1983 to support a four-speaker configuration, Slots 3,4, 6 and 7 must be used for a dual-audio Codec configuration. To configure the ES1983 to support a six-speaker configuration, Slots 3,4,6, 7, 8 and 9 must be used for a triple-audio Codec configuration.

Contact your ESS FAE for complete details on implementing multiple audio Codec configurations into your planned audio subsystem designs.
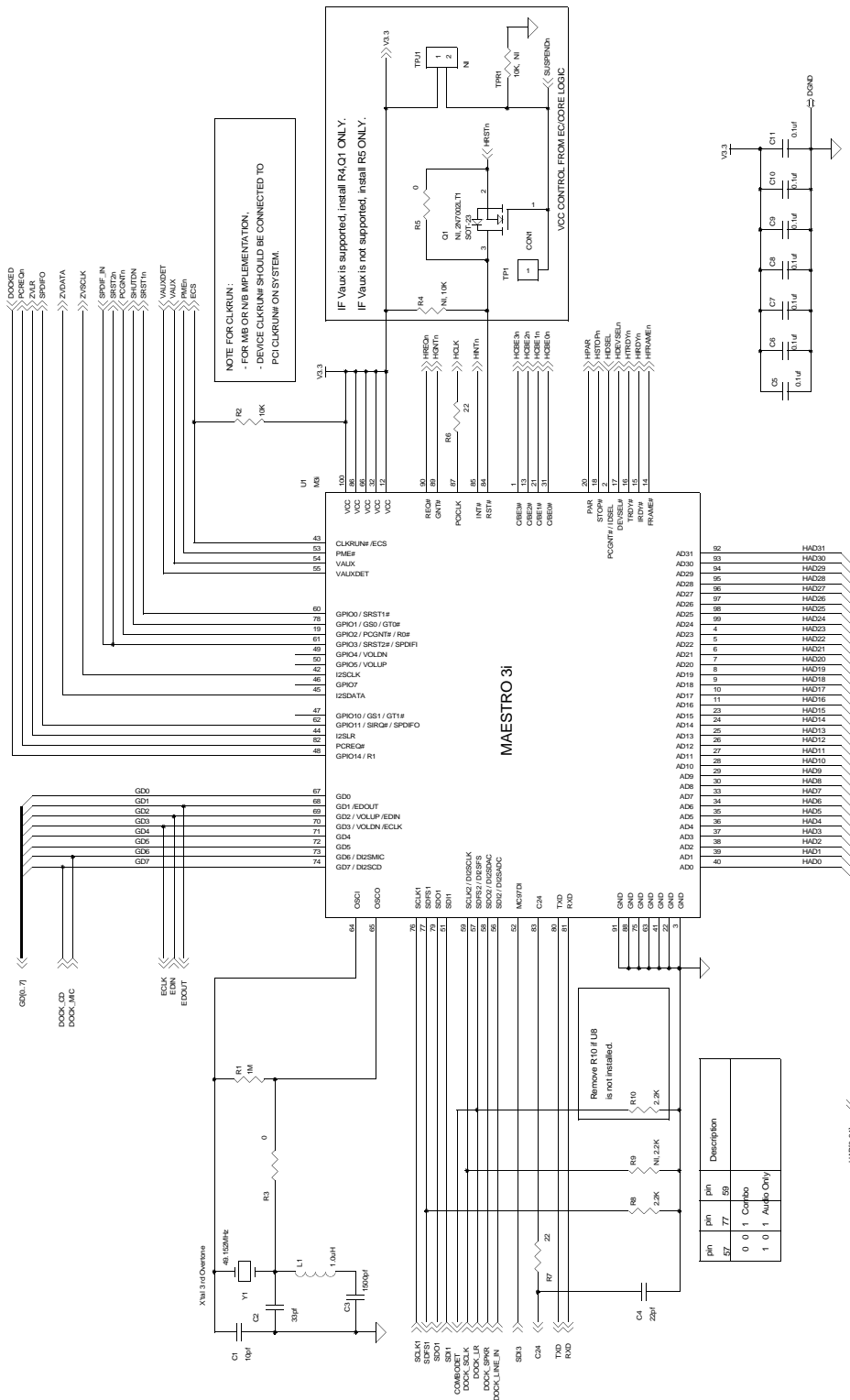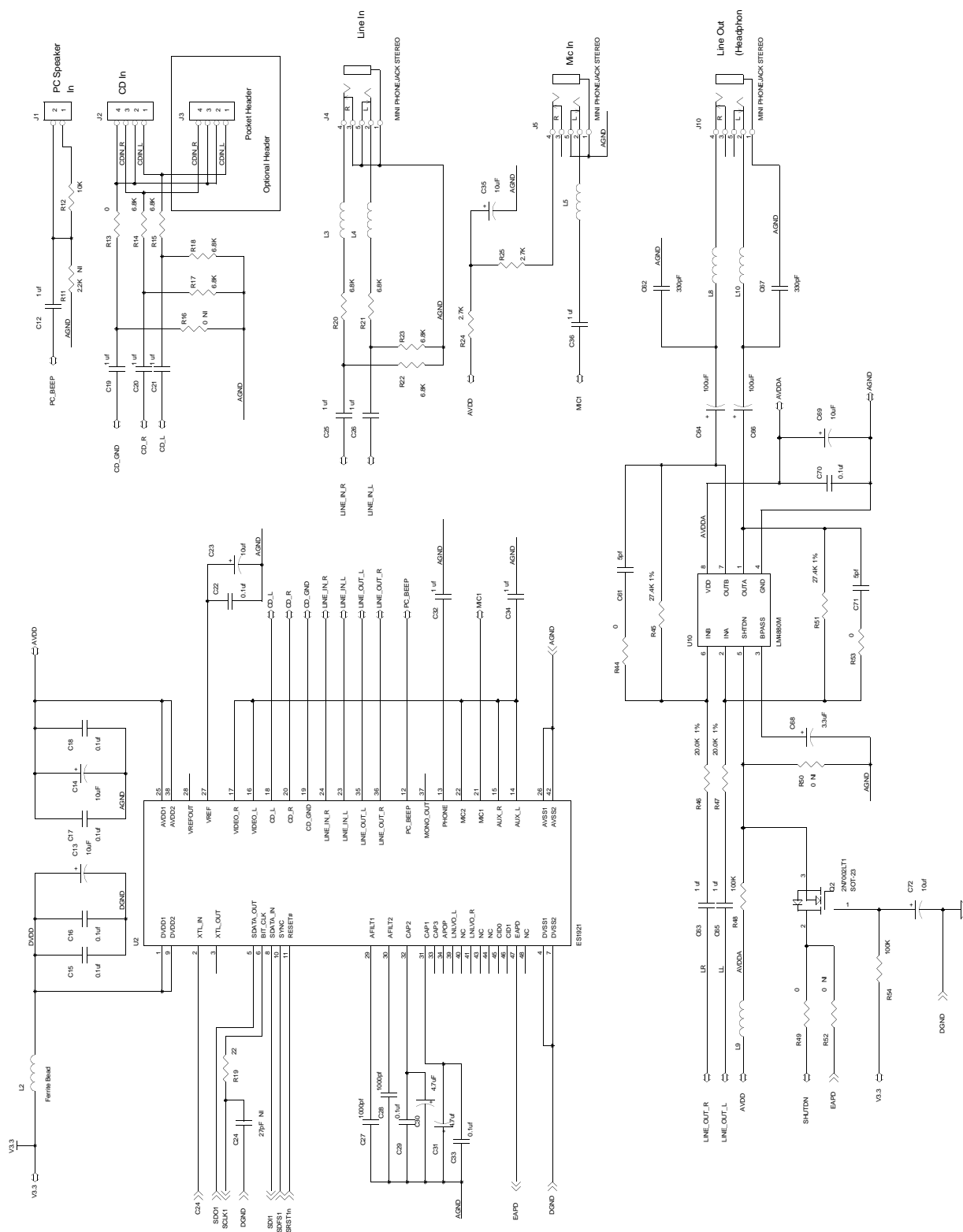
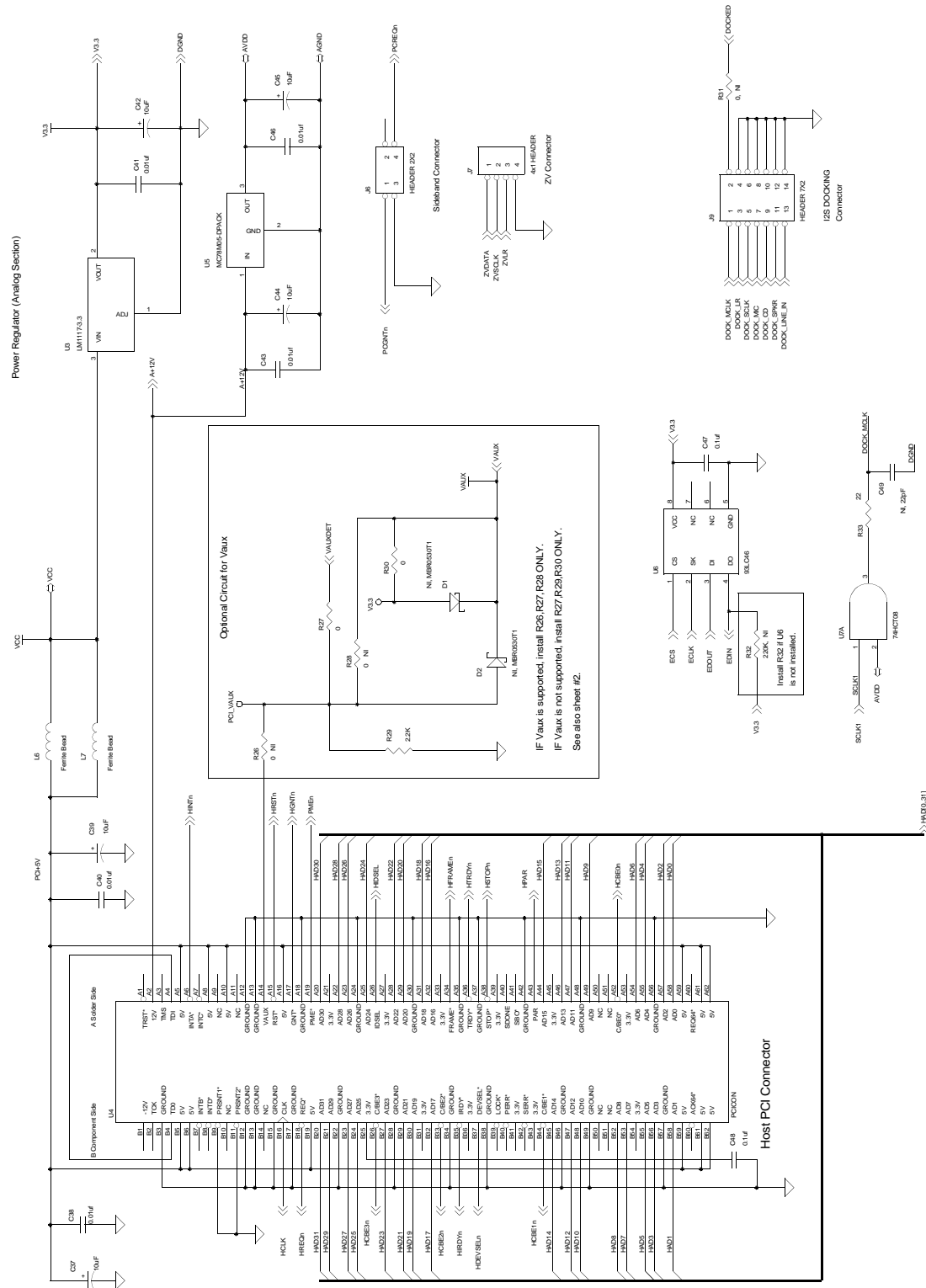# APPENDIX A: SCHEMATIC EXAMPLES
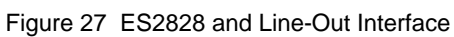

Figure 24 ES1983 Maestro-3i

Figure 25 ES1921 AC'97 Codec Interface

Figure 26 PCI Bus Interface

COMPANY CONFIDENTIAL

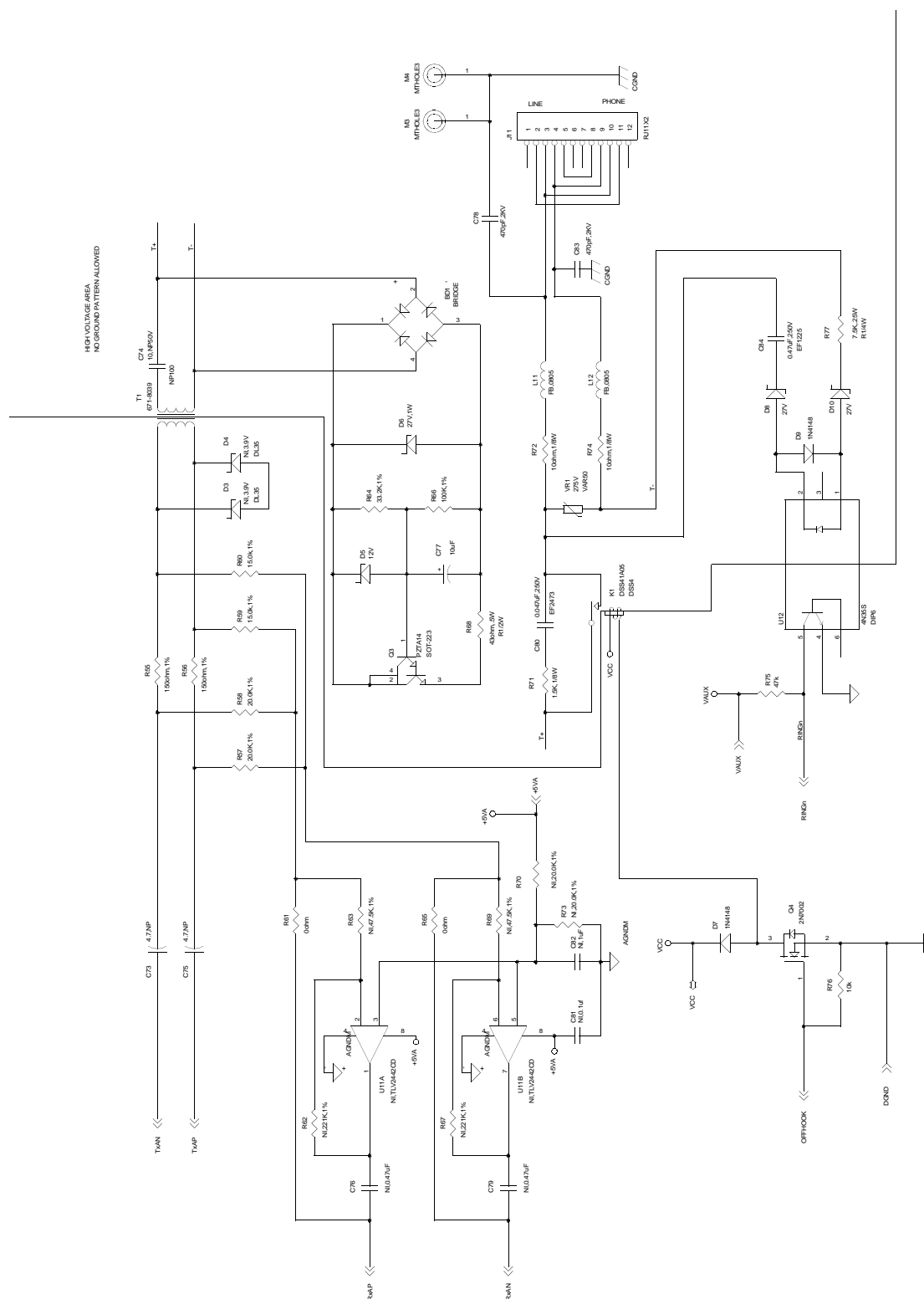Figure 27 ES2828 and Line-Out Interface

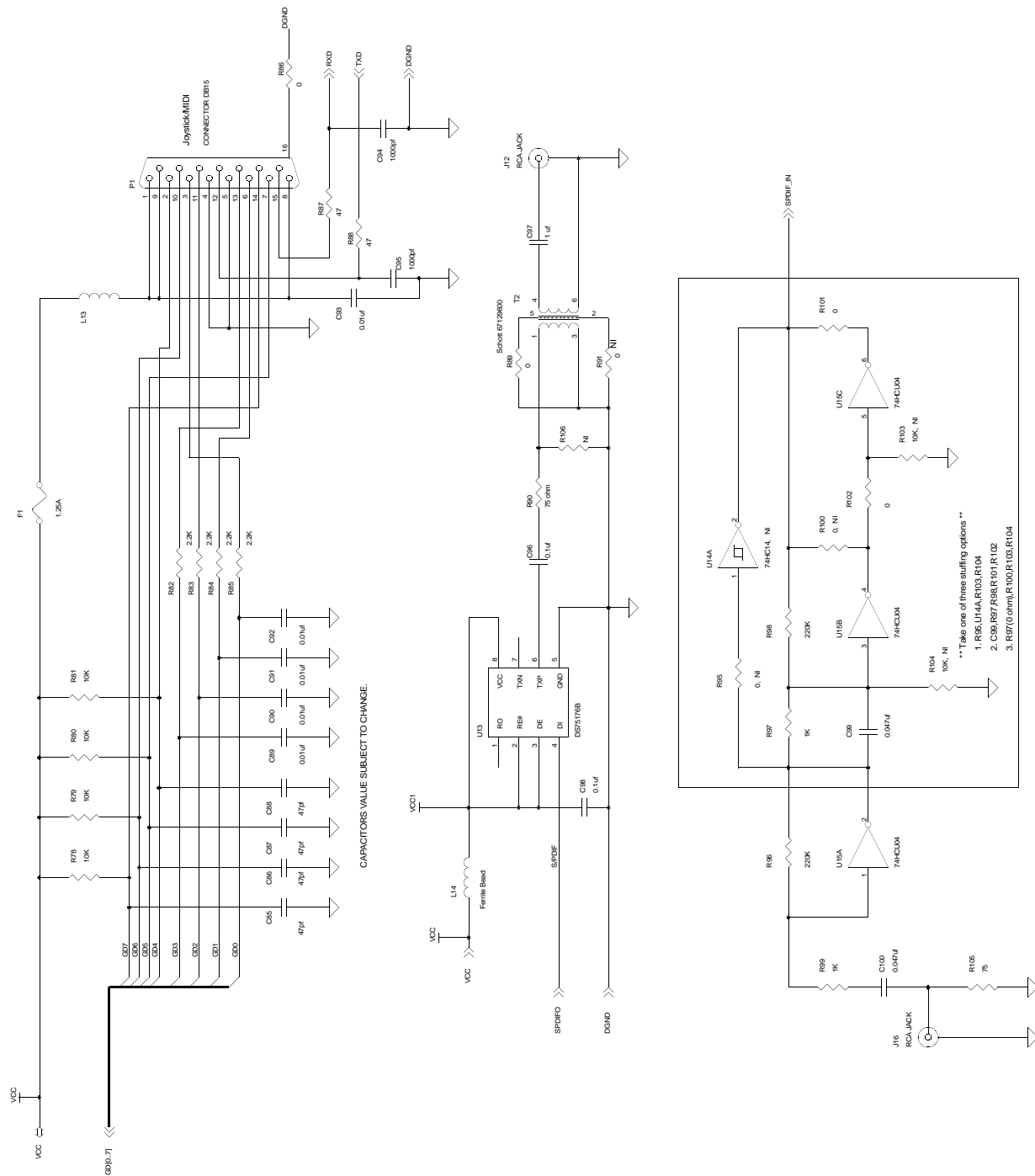Figure 28 Modem DAA Interface

Figure 29 MIDI and S/PDIF Interface

APPENDIX B: BILL OF MATERIALS

(NOTEBOOK WITH V$_{AUX}$ SUPPORT)

Item	Component Description	Qty	Reference Designator
1	Xtal, 49.152MHz, 3rd Overtone, 100ppm, 10pf, 40ohm, HC-49/U	1	Y1
2	M3i ES1983S 100 pins TQFP	1	U1
3	ES2828S Modem AFE 48 pins TQFP	1	U8
4	ES1921(AC97), 48PQFP	1	U2
5	DS75176B, Transceivers	1	U13
6	78L05, TO-92	2	U5,U9
7	LM1117-3.3	1	U3
8	LM4880M, 250mW Stereo Audio Power Amplifier	1	U10
9	74HCT08	1	U7
10	SCHOTT-67129600, Transformer, Thro-hole	1	T2
11	Transformer,1:1,600ohm,Midcom 671-8039	1	T1
12	93LC46	1	U6
13	Optocoupler, 4N35, DIP-6	1	U12
14	74HCU04, SOIC	1	U15
15	Varistor,275V 5mm, Harris V275LA4	1	VR1
16	Res, 5%, 0, SMD, 0805	16	R3,R13,R26,R27,R28,R34,R35,R36,R44, R49,R53,R61,R65,R86,R89,R91
17	Res, 5%, 22, SMD, 0805	4	R6,R7,R19,R33
18	Res, 5%, 47, SMD, 0805	2	R87,R88
19	Res, 5%, 110, SMD, 0805	1	R90
20	Res, 5%, 2.2K, SMD, 0805	6	R8,R10,R82,R83,R84,R85
21	Res, 5%, 2.7K, SMD, 0805	2	R24,R25
22	Res, 5%, 6.8K, SMD, 0805	8	R14,R15,R17,R18,R20,R21,R22,R23
23	Res, 5%, 10K, SMD, 0805	16	R2, R4, R12, R39, R40, R41, R42, R43, R76, R78, R79, R80, R81, R94, R101, R102
24	Res, 5%, 47K, SMD, 0805	3	R37,R38,R75
25	Res, 5%, 100K, SMD, 0805	2	R48,R54
26	Res, 5%, 1M, SMD, 0805	1	R1
27	Res, 1%, 150.0, SMD, 0805	2	R55,R56
28	Res, 1%, 15.0K, SMD, 0805	2	R59,R60
29	Res, 1%, 20.0K, SMD, 0805	4	R46,R47,R58,R57
30	Res, 1%, 27.4K, SMD, 0805	2	R45,R51
31	Res, 1%, 33.2K, SMD, 0805	1	R64
32	Res, 1%, 100.0K, SMD, 0805	1	R66
33	Res, 5%, 10, 1/8W, SMD, 0805	2	R72,R74
34	Res, 5%, 43, 1/2W, Axial	1	R68
35	Res, 5%, 1.5K, 1/8W, SMD, 0805	1	R71
36	Res, 5%, 7.5K, 1/4W, Axial	1	R77
37	Res, 5%, 75, SMD, 0805	1	R105
38	Res, 5%, 1K, SMD, 0805	2	R97, R99
39	Res, 5%, 220K, SMD, 0805	2	R96, R98
40	Cap, Cera, SMD, 10%, 25V, 5pf, 0805	2	C61,C71
41	Cap, Cera, SMD, 5%, 50V, 10pf, 0805	1	C1
42	Cap, Cera, SMD, 5%, 50V, 22pf, 0805	1	C4
43	Cap, Cera, SMD, 5%, 50V, 33pf, 0805	1	C2
44	Cap, Cera, SMD, 5%, 50V, 47pf, 0805	4	C85,C86,C87,C88
45	Cap, Cera, SMD, 5%, 50V, 330pf, 0805	2	C62,C67
46	Cap, Cera, SMD, 10%, 50V, 1000pf, 0805	4	C27,C28,C94,C95
47	Cap, Cera, SMD, 10%, 50V, 1500pf, 0805	1	C3
44	Cap, Cera, SMD, 10%, 50V, 0.01μf, 0805	10	C38, C40, C41, C43, C46, C89, C90, C91, C92, C93

45	Cap, Cera, SMD, 10%, 50V, 0.1µf, 0805	27	C5,C6,C7,C8,C9,C10,C11,C15,C16,C17, C18,C22,C29,C33,C47,C48,C50,C51,C52, C53,C55,C56,C58,C60,C70,C96,C98
46	Cap, Cera, SMD, 10%, 50V, 1µf, 0805	12	C12,C19,C20,C21,C25,C26,C32,C34,C36, C63,C65,C97
47	Cap,Radial 20%,25V, 3.3µf, Size .100"	1	C68
48	Cap,Radial 20%,25V, 4.7µf, Size .100"	2	C30,C31
49	Cap,Radial 20%,25V, 10µf, Size .100"	15	C13,C14,C23,C35,C37,C39,C42,C44,C45, C54,C57,C59,C69,C72,C77
50	Cap,Radial 20%,25V, 100µf, Size .100"	2	C64,C66
51	Cap, Disc, 10%, 2KV, 470pF	2	C78,C83
52	Cap, Mploy, 20%, 250V, 0.047µf, Ra-0.3sp	1	C80
53	Cap, Mploy, 20%, 250V, 0.47µf, Ra-0.6sp	1	C84
54	Cap, NP Elec, 20%, 50V, 4.7µf, Ra-0.1sp	2	C73,C75
55	Cap, NP Elec, 20%, 50V, 10µf, Ra-0.1sp	1	C74
56	Cap, Cera, SMD, 10%, 50V, 0.047µf, 0805	2	C99, C100
57	Diode,Zener,12V,SOD-80	1	D5
58	Diode,Zener,27V,1W,MELF	1	D6
59	Diode,Zener,27V,SOD-80	2	D8,D10
60	Diode,Signal,100V,SOD-80,1N4148	2	D7,D9
61	Bridge Rectifier, W04G	1	BD1
62	Relay,SPST,Form 1A, DSS41A05	1	K1
63	Ferrite Bead, TDK (CB30 – 0805), 0805	7	L3,L4,L5,L8,L10,L11,L12
64	High Current Bead, CTC (HH-1H3216-500),1206	6	L2,L6,L7,L9,L13,L14
65	Inductor, 1.0uH, SMD, 1210	1	L1
66	Fuse, 1.25A, Thru-hole	1	F1
67	2N7002LT1, SOT-23, TMOS FET Transistor	1	Q1
68	2N7002LT1, SOT-23, TMOS FET Transistor	2	Q2,Q4
69	Darlington Transistor,NPN, PZTA1a,SOT223	1	Q3
70	RCA JACK	2	J12, J16
71	Mini stereo jack connector, 5 pin,SJ372N	2	J5,J6
72	Mini stereo jack connector, 5 pin,SJ372	1	J10
73	2mm Wafer Socket, 4 pin	1	J2
74	DB15 female connector (right angle)	1	P1
75	MDC P30, AMP 3-179397-0	1	J13
76	Dual RJ-11 Jack,Millennium, AJ026-16-2-4	1	J11
77	HEADER 2X1	1	J1
78	HEADER 3X1	2	J14,J15
79	HEADER 4X1	1	J7
80	HEADER 2X2	1	J6
81	HEADER 7X2	1	J9
82	SHUNT, 2.54mm	2	J14,J15

ORDERING INFORMATION

Part Number	Package
ES1983S	100-pin TQFP

ESS Technology, Inc.
48401 Fremont Blvd.
Fremont, CA 94538
Tel: 510-492-1088
Fax: 510-492-1098

AudioDrive®

No part of this publication may be reproduced, stored in a retrieval system, transmitted, or translated in any form or by any means, electronic, mechanical, manual, optical, or otherwise, without the prior written permission of ESS Technology, Inc.

ESS Technology, Inc. makes no representations or warranties regarding the content of this document.

All specifications are subject to change without prior notice.

ESS Technology, Inc. assumes no responsibility for any errors contained herein.

(P) U.S. Patent 4,214,125 and others, other patents pending.

*Audio***Drive**® is a registered trademark of ESS Technology, Inc.

All other trademarks are owned by their respective holders and are used for identification purposes only.